DHCOM I.MX6

User Manual

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THE ART OF INNOVATION

Changes

Version	Date	Changes	Name
1.0	2014-04-04	First version	AG
1.1	2014-05-26	Add E-tec SODIMM connector Add RoHS conformance information	AG
1.2	2014-11-25	Changed VCC (Vin) min. voltage	AG
1.3	2014-11-27	Add DualLite and Solo power consumption (see 5.1) Add table column "Not used" description Changed CAN "IO Type" information (see table 16) Delete USB OTG duplicated table entry (see table 7) Reworked module dimensions (see Figure 8)	AG
1.4	2014-12-02	Add EMI termination note to RGB interface nets (see 3.11.1) Add GPIO Out of reset state (see table 24)	AG
1.5	2015-03-31	Changed the note "DDR2" to "DDR" at SODIMM-200 socket information (see 5.4.1) Add HW coding information (see 3.2) Add reset timings (see 5.2) Add ripple information (see 5.1)	AG
1.6	2015-04-01	Fixed wrong IO type information at table 4 hardware coding	AG
2.0	2015-07-20	Documentation now fits to i.MX6 module with high speed socket (HW300) - Audio codec removed and I2S info add - Add high speed connector documentation - DHCOM I2C interfaces exchanged Add detailed reset description (see 3.1.2) Hardware Coding for future use has changed (see 3.2) Changed LC_EN description form "LCD display enable" to "LCD display data enable"(see 3.12)	AG
R01	2016-02-02	Document Review from HH.	AG
R02	2016-02-18	Add Quad Core power consumption information	AG

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Abbreviations

- AIN = Analog input
- AINOUT = Analog input/output
- I = Input
- IO = Input/output
- MBC = Must be connected
- O = Output
- PD = Pull-Down
- PU = Pull-Up
- PWR_I = Power input
- PWR_O = Power output
- TBD = To be defined

1 Introduction

1.1 Hardware

The DHCM-iMX6-01D2 module is a computer module in the SODIMM-200 form factor on the basis of a Cortex-A9 processor from Freescale. The CPU is clocked up to 1.2 GHz and is equipped with up to 2 GByte DDR3-Memory and 16 GByte eMMC flash. Numerous interfaces are also available for communicating with the outside world, which are required in embedded systems.

The pin assignment of the SODIMM 200 socket and the Molex high speed connector is subject to the DHCOM standard, so that a replacement or an upgrade to other DHCOM modules is very easily possible.

1.2 Software

At present, the DHCM-iMX6-01D2 module is available with the Embedded Linux, Android and Windows Embedded Compact operating systems.

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.

1.3 Main characteristics

- Cortex-A9 Freescale i.MX6 Solo/Dual(Lite)/Quad up to 1.2GHz
- 2D/3D graphics accelerator
- 0 - 512 MByte NAND flash memory (8 bit bus width) or 2 - 16 GByte eMMC flash
- 2 MB SPI boot flash
- 256 - 2048 MByte DDR3-1066 or DDR3-800
- On-board microSD card socket
- SD/MMC card interface, 4 bit SDIO
- LC display controller, 24 bit colors, 1920 x 1200 pixels
- LVDS single and dual channel (single channel: max. 1366 x 768 pixels / dual channel: max. 1920 x 1200)
- HDMI V1.4a 1080p (1920x1080)
- MIPI CSI-2 camera interface (2-data lanes)
- On-board touch controller for 4-wire resistive touch screens
- Ethernet controller 10/100 Mbit, IEEE1588 conform
- RGMII interface for Gbit Ethernet
- USB 2.0 OTG high-speed
- USB 2.0 host high speed
- PCIe 2.0 and 1.1 compliant interface

- Serial ATA Rev. 2.5 compliant interface
- Full function UART
- Standard UART with hardware handshake support
- Standard UART
- CAN interface
- 2 x SPI interface
- 2 x I2C™ interface
- I²S Audio interface
- Real-time clock (I2C™ connection), low power temperature compensated
- 12 bit analog input
- 1 kbit EEPROM with integrated MAC address
- 16 bit address/databus interface on SODIMM-200 socket
- PWM channel
- 23 GPIOs
- JTAG debug connection via FFC plug connector
- Industrial temperature range (-40°C to +85°C)
- SODIMM-200 socket with DHCOM pin assignment
- Molex high speed socket with DHCOM-X pin assignment

1.4 CPU differences

Description	i.MX6 Solo	i.MX6 DualLite	i.MX6 Dual	i.MX6 Quad
Housing	21x21 mm BGA plastic	21x21 mm BGA plastic	21x21 mm BGA metal or bare die package	21x21 mm BGA metal or bare die package
Cores	1x	2x	2x	4x
Cooling	Not necessary	Not necessary	Maybe necessary	Passive cooling necessary
CPU speed	Up to 1GHz	Up to 1GHz	Up to 1.2GHz	Up to 1.2GHz
2D graphics	1x graphic engine	1x graphic engine	2x graphic engine	2x graphic engine
3D graphics	with 1x shader	with 1x shader	with 4x shader	with 4x shader
IPU	1x	1x	2x	2x
Display	2 x WXGA (1366x786)	2 x WXGA (1366x786)	2 x 4XGA (2048x1536)	2 x 4XGA (2048x1536)
Cache	512kB L2 cache	512kB L2 cache	1MB L2 cache	1MB L2 cache
Memory	DDR3-800	DDR3-800	DDR3-1066	DDR3-1066
Sata	-	-	1x	1x

Table 1: CPU differences

1.5 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

1.5.1 Freescale i.MX6 processor

Data sheets and technical documents can be found at http://www.freescale.com/

1.5.2 Microchip ethernet PHY LAN8710Ai

Data sheets and technical documents can be found at https://www.microchip.com/

1.5.3 Micro Crystal real-time clock RV-3029-C3

Data sheets and technical documents can be found at http://www.microcrystal.com/

1.5.4 TI touch controller TSC2014

Data sheets and technical documents can be found at http://www.ti.com/

2 Hardware overview

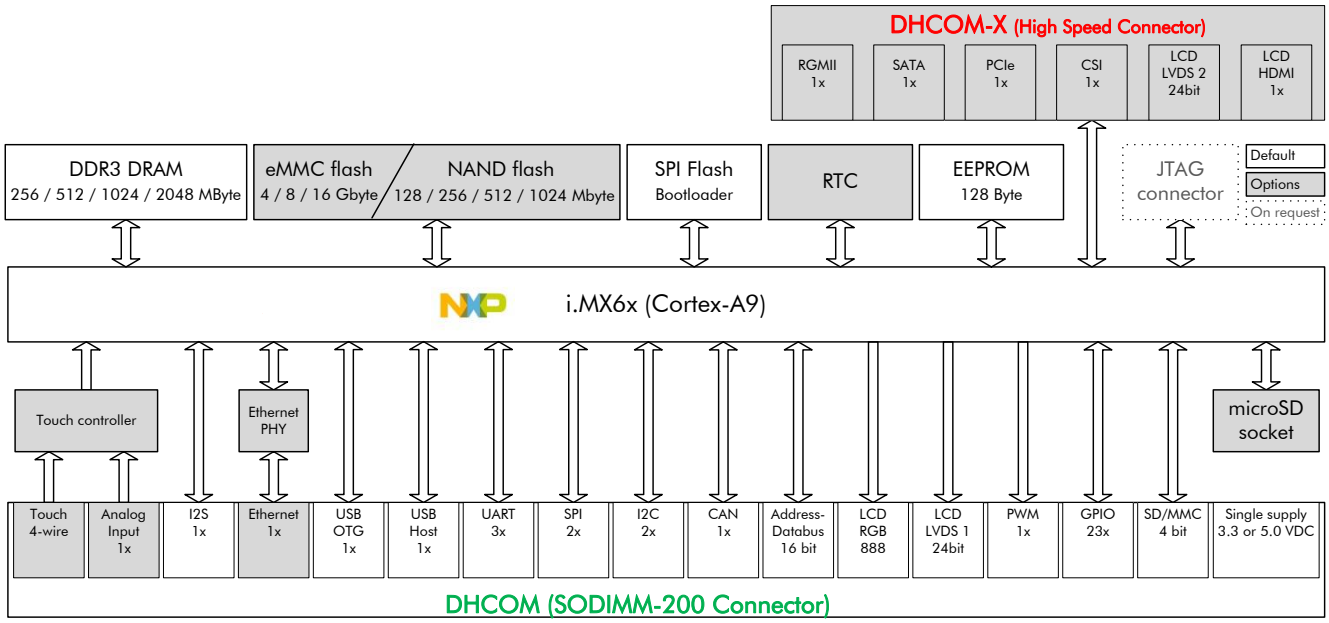


Figure 1: DHCM-iMX6-01D2 block diagram

Figure 1 provides an overview of the DHCM-iMX6-01D2 module. All interfaces and memory components are shown. All grayed blocks could be mounted optional on a specific customer core module.

3 Signal description

The following subsections describe the signals at the SODIMM-200 and Molex high speed socket. The green marked table columns belong to DHCOM SODIMM-200 connector and the red marked to DHCOM-X Molex high speed connector.

Notes:

- For all specified pull-up and pull-down resistors, a value of 10k is recommended.
- "Not used" specification describes, what needs to be done with unconnected pins.

DHCOM hardware compatibility:

The DHCOM specification specifies function groups in order to ensure compatibility between various DHCOM modules. Each function group has its own voltage level output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters on the customer specific main board provide compatibility between various DHCOM modules. Naturally, these level shifters can also be removed from the customer design. In this case, the customer will lose compatibility to the DHCOM standard.

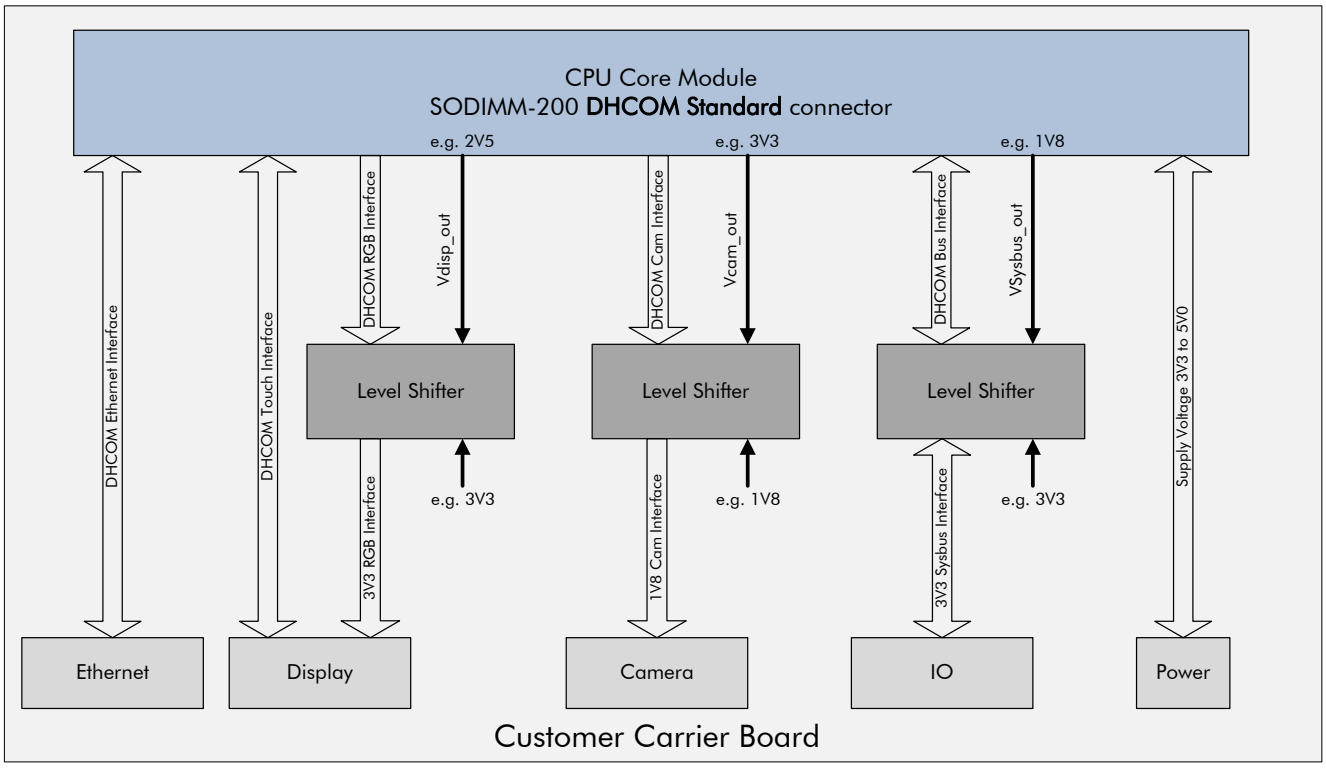


Figure 2: DHCOM functions groups concept

Important:

With the level shifter concept it is possible to support all core modules which are developed from DH electronics in the future. If you only like to use the current DHCOM modules (DHCOM i.MX25, AM35x, i.MX6 and AM335x) you only need to use level shifters in special cases, if you have a look at the following table:

Voltage	i.MX25	AM3517	AM335x	i.MX6
VCC (Vin)	3.2V – 5.5V	3.2V – 5.5V	3.2V – 5.5V	3.2V – 5.5V
Vbat	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V
Vsysbus	1.8V	3.3V	-	3.3V
Vdisp	3.3V	3.3V	3.3V	3.3V
Vcam	3.3V	3.3V	3.3V	3.3V
VIO	3.3V	3.3V	3.3V	3.3V
VETH_VIO_SWITCHED	3.3V	3.3V	3.3V	3.3V
VCC_RGMII_OUT	-	-	3.3V	2.5V

Table 2: Voltage groups

Summary:

At the moment you only need level shifters at address and data bus interface, if you like to use parallel address and data bus, i.MX25 and another DHCOM core module in the same mainboard hardware.

3.1 Power supply and reset

3.1.1 Power supply

The DHCM-iMX6-01D2 has the following power connections:

- Vin = Core module supply voltage input
- Vbat = Battery voltage input
- Vsysbus = System bus voltage output
- Vdisp = Display voltage output
- Vcam = Camera voltage output
- VIO = I/O voltage output
- VCC_RGMII_OUT = Supply voltage for Gbit PHY IO voltage

Note: When no buffer battery is used in the system, Vbat must be connected with 3.3V.

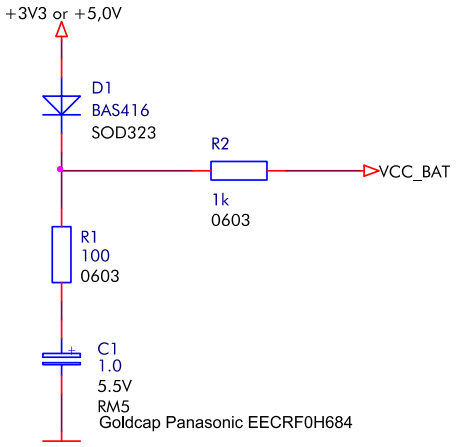


Figure 3: Vbat GoldCap example

The power supply connections Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT are to be used to detect the right voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with the level shifter.

3.1.2 Reset

The System is put in reset state by holding RESET_IN signal low.

When the RESET_IN is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_OUT are asserted as long as RESET_IN is asserted. If the reset input RESET_IN is de-asserted, the RESET_OUT is also de-asserted and the module starts booting again.

It is not necessary to held RESET_IN low during power-up.

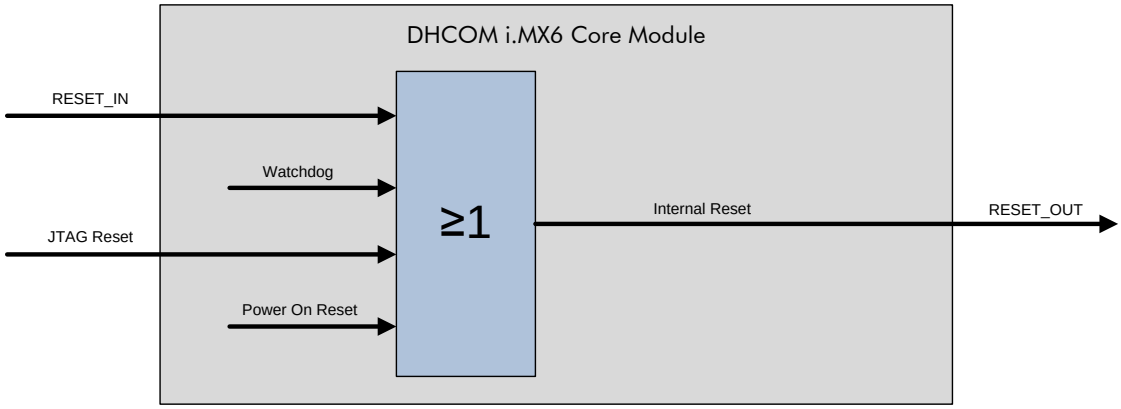


Figure 4: Reset

3.1.3 Signal Overview

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
VCC_IN1	Core Module supply voltage input	38	PWR_I	-	MBC
VCC_IN2	Core Module supply voltage input	39	PWR_I	-	MBC
VCC_IN3	Core Module supply voltage input	40	PWR_I	-	MBC
VCC_IN4	Core Module supply voltage input	41	PWR_I	-	MBC
VCC_IN5	Core Module supply voltage input	42	PWR_I	-	MBC
VCC_IN6	Core Module supply voltage input	44	PWR_I	-	MBC
GND1	Core Module Ground	17	PWR_I	-	MBC
GND2	Core Module Ground	19	PWR_I	-	MBC
GND3	Core Module Ground	43	PWR_I	-	MBC
GND4	Core Module Ground	45	PWR_I	-	MBC
GND5	Core Module Ground	47	PWR_I	-	MBC
GND6	Core Module Ground	101	PWR_I	-	MBC
GND7	Core Module Ground	111	PWR_I	-	MBC
GND8	Core Module Ground	153	PWR_I	-	MBC
GND9	Core Module Ground	185	PWR_I	-	MBC
GND10	Core Module Ground	199	PWR_I	-	MBC
VCC_BAT	Core Module Battery voltage input	200	PWR_I	-	MBC
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	-	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	-	MBC
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
Vcam_OUT	Camera supply voltage output	102	PWR_O	-	-
VIO_OUT	I/O supply voltage output	152	PWR_O	-	-
RESET_IN	System Reset input (active low)	21	I	-	-
RESET_OUT	System Reset output (active low)	20	O	-	-

Table 3: SODIMM-200 Power supply and reset

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
VCC_IN7	Core Module supply voltage input	79	PWR_I	-	MBC
VCC_IN8	Core Module supply voltage input	80	PWR_I	-	MBC
GND11	Core Module Ground	19	PWR_I		MBC
GND12	Core Module Ground	22	PWR_I		MBC
GND13	Core Module Ground	25	PWR_I		MBC
GND14	Core Module Ground	28	PWR_I		MBC
GND15	Core Module Ground	35	PWR_I	-	MBC
GND16	Core Module Ground	36	PWR_I	-	MBC
GND17	Core Module Ground	41	PWR_I	-	MBC
GND18	Core Module Ground	46	PWR_I	-	MBC
GND19	Core Module Ground	53	PWR_I	-	MBC
GND20	Core Module Ground	58	PWR_I	-	MBC
GND21	Core Module Ground	67	PWR_I	-	MBC
GND22	Core Module Ground	68	PWR_I	-	MBC
VCC_RGMII_OUT	2,5V Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	-	-

Table 4: DHCOM-X Power supply

3.2 Hardware coding

The following pins can be used to read out the current hardware version of the DHCOM i.MX6 core module.

CPU ball name	Description	CPU ball number	IO Type
EIM_A19	Code_HW_0	G25	I
EIM_A23	Code_HW_1	J21	I
EIM_A22	Code_HW_2	F24	I

Table 5: Hardware coding

DH PCB Numbers	Description	Code_HW_2	Code_HW_1	Code_HW_0
493-100, 493-200	DHCOM i.MX6 without High Speed Interfaces	0 (100k PD)	0 (100k PD)	0 (100k PD)
493-300 **(current version)**	DHCOM i.MX6 with High Speed Interfaces	0 (100k PD)	0 (100k PD)	1 (100k PU)
493-400		0 (100k PD)	1 (100k PU)	0 (100k PD)
493-500		0 (100k PD)	1 (100k PU)	1 (100k PU)
493-600		1 (100k PU)	0 (100k PD)	0 (100k PD)
…		…	…	…

Table 6: Different hardware versions

3.3 Touch controller / Analog inputs

The DHCM-iMX6-01D2 module is equipped with a 4-Wire 12 bit resistive Touch Controller (Texas Instruments TSC2014), which is connected via I2C™ with the iMX6 processor. In addition, this touch controller offers an analog input for, e.g. temperature or voltage measurements, which is also administered on the SODIMM-200 connections.

I2C™ device address of the touch controller: 0x49

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments. http://www.ti.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
TSPX	Resistive Touch: 4 wire (X +)	12	AINOUT	-	PD
TSMX	Resistive Touch: 4 wire (X -)	14	AINOUT	-	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	AINOUT	-	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	AINOUT	-	PD

Table 7: Touch controller connections

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
Analog_In0	Analog input 0	8	AIN	-	PD

Table 8: Analog inputs

3.4 Ethernet

The iMX6 processor includes a 10/100/1000 Ethernet Media Access Controller (MAC). A 10/100 Ethernet transceiver (Microchip LAN8710Ai) is connected on the module at this interface. This Ethernet interface fulfils the IEEE 802.3 standard.

For more precise information, we refer here to the data sheet and other technical documents of Freescale and Microchip.

http://www.freescale.com/

https://www.microchip.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	-	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	-	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	-	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	-	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	-	-
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	-	PD
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	-	PD

Table 9: Ethernet connections

Note: The LED outputs "nETH1_LINK_LED" and "nETH1_SPEED_LED" must be connected as follows:

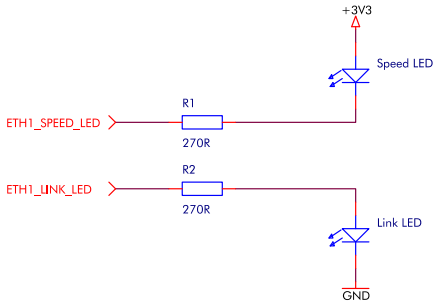


Figure 5: Ethernet LED circuitry

Note: In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration lines.

3.5 USB

The DHCM-iMX6-01D2 module supports a maximum of two USB devices. These consist of a USB OTG connection and one USB host connection. For both connections the integrated iMX6 PHYs are used.

All two ports are high-speed USB connections, which also support full speed and low speed.

3.5.1 USB OTG

This USB interface fulfils the USB 2.0 specification. It can be configured as OTG, host or device. As a host, it supports peripheral devices of all speeds and as a peripheral, it communicates at either high-speed (480Mbps) or full speed (12Mbps) when connected to legacy host computers.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_OTG_VBUS	OTG Client: VBUS Input line OTG Host: USB bus supply voltage	166	I / PWR_O	-	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	-	-
USB_OTG_D+	USB OTG differential Signal positive line	170	IO	-	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	IO	-	PD

Table 10: USB OTG

Note: The DHCOM USB OTG port does not provide any "enable" and "over current" signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event, the "over current" output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

3.5.2 USB Host

The USB Host 1 port fulfils the USB 2.0 specification. It supports high-speed, full speed and low speed data transfers.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_PWR_STAT	USB Host over current indicator (active low)	174	I	-	-
USB_PWR_EN	USB Host power enable signal (active low)	176	O	-	-
USB_HOST_D1+	USB Host differential Signal positive line	178	IO	-	PD
USB_HOST_D1-	USB Host differential Signal negative line	180	IO	-	PD

Table 11: USB Host

3.6 UART

The DHCM-iMX6-01D2 module offers connections for a total of three UARTs. UART 1 and UART 2 additionally support a hardware handshake.

The maximum transfer rate is 5 Mbit/s.

For more precise information, we refer here to the data sheet and other technical documents of Freescale.

http://www.freescale.com/

3.6.1 UART 1

Note: DHCOM UART 1 is the UART 1 module of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART1_DTR	Full function UART data terminal ready	22	O	EIM_D24	-
UART1_CTS	UART clear to send	24	I	EIM_D20	-
UART1_RTS	UART request to send	26	O	EIM_D19	-
UART1_DSR	Full function UART data set ready	28	I	EIM_D25	-
UART1_DCD	Full function UART data carrier detect	30	I	EIM_D23	-
UART1_RX	UART receive data line	32	I	SD3_DAT6	-
UART1_TX	UART transmit data line	34	O	SD3_DAT7	-
UART1_RI	Full function UART ring indicator	36	I	EIM_EB3	-

Table 12: UART 1

Hardware design notes: It is essential to always create a possible connection to DHCOM UART 1, since the DHCOM bootloader can be operated with the UART 1. A minimum connection possibility should be made available via solder pads.

3.6.2 UART 2

Note: DHCOM UART 2 is the UART 5 module of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART2_CTS	UART clear to send	31	I	CSI0_DAT18	-
UART2_RTS	UART request to send	33	O	CSI0_DAT19	-
UART2_RX	UART receive data line	35	I	CSI0_DAT15	-
UART2_TX	UART transmit data line	37	O	CSI0_DAT14	-

Table 13: UART 2

3.6.3 UART 3

Note: DHCOM UART 3 is the UART 4 module of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART3_RX	Serial port receive data line	23	I	CSI0_DAT13	-
UART3_TX	Serial port transmit data line	25	O	CSI0_DAT12	-

Table 14: UART 3

3.7 Serial port interface

The DHCM-iMX6-01D2 module is equipped with two SPI interfaces. These interfaces consist of a full duplex capable, 4-wire interface and have the following characteristics:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable

- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

For more precise information, we refer here to the data sheet and other technical documents of Freescale.

http://www.freescale.com/

3.7.1 SPI 1

Notes:

- DHCOM SPI Port 1 is connected to the ECSPI1 interface of the i.MX6
- SPI1_CS0 on the SODIMM-200 socket uses the ECSPI1_SS2 signal of the i.MX6
- The ECSPI1 interface of the i.MX6 is also used for the on-board SPI flash
- ECSPI1_SS0 is used for the on-board SPI flash

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SPI1_CS0	Slave select signal	177	O	KEY_ROW2	-
SPI1_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	EIM_D16	-
SPI1_MISO	SSP receive data line	181	I	EIM_D17	-
SPI1_MOSI	SSP transmit data line	183	O	EIM_D18	-

Table 15: SPI1 Interface

3.7.2 SPI 2

Notes:

- DHCOM SPI Port 2 is connected to the ECSPI2 interface of the i.MX6
- SPI2_CS0 on the SODIMM-200 socket uses the ECSPI2_SS0 signal of the i.MX6

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SPI2_CS0	Slave select signal	155	O	CSI0_DAT11	-
SPI2_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	157	IO	CSI0_DAT8	-
SPI2_MISO	SSP receive data line	159	I	CSI0_DAT10	-
SPI2_MOSI	SSP transmit data line	161	O	CSI0_DAT9	-

Table 16: SPI2 Interface

3.8 I²C™

The DHCM-iMX6-01D2 module provides the opportunity to connect up to two separate I²C™ multimaster buses. The I²C™ bus controller integrated in the i.MX6 has the following main features:

- Compatibility with I2C bus standard
- Multiple-master operation
- Software-programmable for one of 64 different serial clock frequencies

- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

The pull-up resistors required according to the I2CTM specification are already fitted on the module. For detailed information about I2CTM, reference is made to the specification (Philips Semiconductor):

http://www.nxp.com

3.8.1 I2C1

Note: DHCOM I2C1 uses the I2C1 instance of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2C1_CLK	I²C clock line	182	IO	KEY_COL3	-
I2C1_DATA	I²C data line	184	IO	KEY_ROW3	-

Table 17: I2C1 Interface

3.8.2 I2C2

Note: DHCOM I2C2 uses the I2C2 instance of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2C2_CLK	I²C clock line	158	IO	EIM_D21	-
I2C2_DATA	I²C data line	160	IO	EIM_D28	-

Table 18: I2C2 Interface

3.8.3 I2C3

Note: The I2C3 instance (I2C_SCL: GPIO_3; I2C_DAT: GPIO_6) of the i.MX6 is used on the core module for the following modules:

- RTC EEPROM (7 bit address: 0x50)
- RTC (7 bit address: 0x56)
- PMIC (7 bit address: 0x3C)
- Touch controller (7 bit address: 0x49)

3.9 CAN

The i.MX6 processor has an integrated standard resp. high-end CAN controller with the following characteristics:

- Supports CAN protocol version 2.0B
- Standard data and remote frames
- Extended data and remote frames
- Zero to eight bytes data length
- Programmable bit rate up to 1 Mb/sec
- Content-related addressing
- Flexible Mailboxes of eight bytes data length
- Each Mailbox is configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Mailbox
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Transmission abort capability
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128
- 100% backwards compatibility with previous FLEXCAN version
- …

Note: DHCOM CAN uses the FLEXCAN1 instance of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
CAN_TX	CAN transmit data line	27	O	KEY_COL2	-
CAN_RX	CAN receive data line	29	I	GPIO_8	-

Table 19: CAN Interface

3.10 Audio Interface

The DHCM-iMX6-01D2 module is equipped with one I2S interface for audio codec connection. This interface has the following characteristics:

- Support for I2S master mode
- Maximum audio sampling rate of 196kHz
- Compliant to Inter-IC Sound (I2S) bus specification from Philips

For more precise information, we refer here to the data sheet and other technical documents of Freescale.

http://www.freescale.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2S_RXD	Data receive signal	5	I	CSI0_DAT7	PD
I2S_TXFS	Transmit Frame sync signal	11	O	CSI0_DAT6	-
I2S_TXD	Data transmit signal	15	O	CSI0_DAT5	-

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2S_TXC	Transmit clock signal	13	O	CSI0_DAT4	-

Table 20: Audio interface

Note: If the audio inputs are not used, they must be closed with a pull-down. The resistor must be connected with VSSA_Audio.

3.11 Address and data bus

The DHCM-iMX6-01D2 module supports the connection of peripheral devices via a parallel address and data bus, by using the i.MX6 EIM bus interface (External Interface Module).

A more precise description for this interface is available in the reference manual of the freescale:

http://www.freescale.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-	-
A00	Memory controller address line	113	O	Latch: EIM_DA0	-
A01	Memory controller address line	115	O	Latch: EIM_DA1	-
A02	Memory controller address line	117	O	Latch: EIM_DA2	-
A03	Memory controller address line	119	O	Latch: EIM_DA3	-
A04	Memory controller address line	121	O	Latch: EIM_DA4	-
A05	Memory controller address line	123	O	Latch: EIM_DA5	-
A06	Memory controller address line	125	O	Latch: EIM_DA6	-
A07	Memory controller address line	127	O	Latch: EIM_DA7	-
A08	Memory controller address line	112	O	Latch: EIM_DA8	-
A09	Memory controller address line	114	O	Latch: EIM_DA9	-
A10	Memory controller address line	116	O	Latch: EIM_DA10	-
A11	Memory controller address line	118	O	Latch: EIM_DA11	-
A12	Memory controller address line	120	O	Latch: EIM_DA12	-
A13	Memory controller address line	122	O	Latch: EIM_DA13	-
A14	Memory controller address line	124	O	Latch: EIM_DA14	-
A15	Memory controller address line	126	O	Latch: EIM_DA15	-
D00	Memory controller data line	135	IO	EIM_DA0	-
D01	Memory controller data line	137	IO	EIM_DA1	-
D02	Memory controller data line	139	IO	EIM_DA2	-
D03	Memory controller data line	141	IO	EIM_DA3	-
D04	Memory controller data line	143	IO	EIM_DA4	-
D05	Memory controller data line	145	IO	EIM_DA5	-
D06	Memory controller data line	147	IO	EIM_DA6	-
D07	Memory controller data line	149	IO	EIM_DA7	-
D08	Memory controller data line	136	IO	EIM_DA8	-
D09	Memory controller data line	138	IO	EIM_DA9	-
D10	Memory controller data line	140	IO	EIM_DA10	-
D11	Memory controller data line	142	IO	EIM_DA11	-
D12	Memory controller data line	144	IO	EIM_DA12	-
D13	Memory controller data line	146	IO	EIM_DA13	-
D14	Memory controller data line	148	IO	EIM_DA14	-
D15	Memory controller data line	150	IO	EIM_DA15	-

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
CS_A	Static memory chip select 0	128	O	EIM_CS0	-
CS_B	Static memory chip select 1	129	O	EIM_CS1	-
WE	Memory controller write enable	133	O	EIM_RW	-
OE	Memory controller output enable	134	O	EIM_OE	-

Table 21: Address and data bus

In Figure 6 the connection between the CPU and the connector is illustrated.

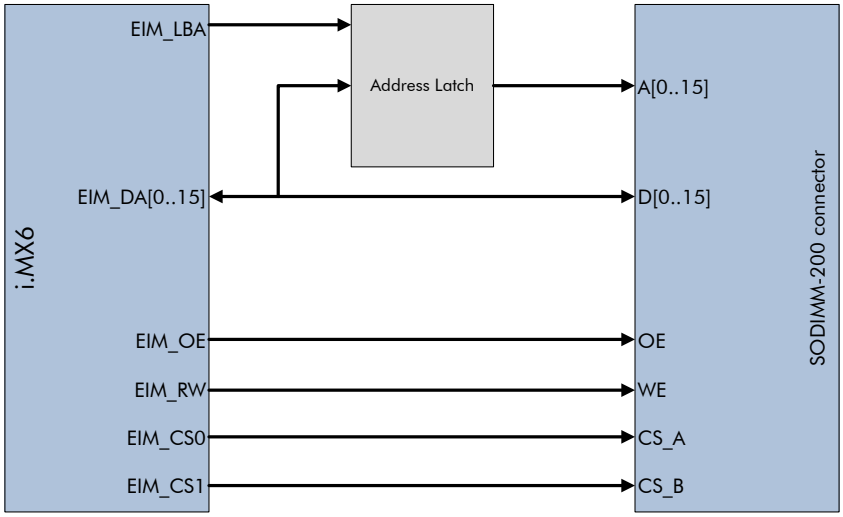


Figure 6: Address and data bus connection to CPU

3.12 Display

3.12.1 RGB

The DHCM-iMX6-01D2 module enables the connection of a 24 bit LCD display. Active as well as passive LCD displays with a resolution of up to 2048 x 1536 pixels can be operated. A parallel RGB888 interface can be used for connection to the display.

The core of the LCD controller is the integrated display subsystem in the i.MX6. More precise information about this is available in the i.MX6 Reference Manual:

http://www.freescale.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
LC_R0	LCD display data red 0	76	O	DISP0_DAT16	- (*)
LC_R1	LCD display data red 1	78	O	DISP0_DAT17	- (*)
LC_R2	LCD display data red 2	49	O	DISP0_DAT18	- (*)
LC_R3	LCD display data red 3	51	O	DISP0_DAT19	- (*)
LC_R4	LCD display data red 4	53	O	DISP0_DAT20	- (*)
LC_R5	LCD display data red 5	55	O	DISP0_DAT21	- (*)
LC_R6	LCD display data red 6	57	O	DISP0_DAT22	- (*)

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
LC_R7	LCD display data red 7	59	O	DISP0_DAT23	- (*)
LC_G0	LCD display data green 0	80	O	DISP0_DAT8	- (*)
LC_G1	LCD display data green 1	82	O	DISP0_DAT9	- (*)
LC_G2	LCD display data green 2	61	O	DISP0_DAT10	- (*)
LC_G3	LCD display data green 3	63	O	DISP0_DAT11	- (*)
LC_G4	LCD display data green 4	65	O	DISP0_DAT12	- (*)
LC_G5	LCD display data green 5	67	O	DISP0_DAT13	- (*)
LC_G6	LCD display data green 6	69	O	DISP0_DAT14	- (*)
LC_G7	LCD display data green 7	71	O	DISP0_DAT15	- (*)
LC_B0	LCD display data blue 0	84	O	DISP0_DAT0	- (*)
LC_B1	LCD display data blue 1	86	O	DISP0_DAT1	- (*)
LC_B2	LCD display data blue 2	73	O	DISP0_DAT2	- (*)
LC_B3	LCD display data blue 3	75	O	DISP0_DAT3	- (*)
LC_B4	LCD display data blue 4	77	O	DISP0_DAT4	- (*)
LC_B5	LCD display data blue 5	79	O	DISP0_DAT5	- (*)
LC_B6	LCD display data blue 6	81	O	DISP0_DAT6	- (*)
LC_B7	LCD display data blue 7	83	O	DISP0_DAT7	- (*)
LC_EN	LCD display data enable	85	O	DI0_PIN15	- (*)
LC_VSYNC	LCD frame or vertical sync. puls	87	O	DI0_PIN3	- (*)
LC_HSYNC	LCD line or horizontal sync. puls	89	O	DI0_PIN2	- (*)
LC_PCLK	LCD pixel clock	91	O	DI0_DISP_CLK	- (*)
GPIO_PWM	LCD contrast (only if PWM is not used)	100	O	SD1_DAT3	-

Table 22: RGB Interface

Note: (*) Regarding EMC it is recommended to terminate RGB interface lines with PD resistor.

3.12.2 LVDS channel 1

The DHCM-iMX6-01D2 module enables the connection of a single link 6bit or 8bit LVDS display. The LVDS standards allow a maximum pixel clock of 112 MHz, which suffices for a display resolution of 1366 x 768 (WXGA) at 60 Hz refresh.

The LVDS display bridge is integrated in the i.MX6. More precise information about this is available in the i.MX6 Reference Manual:

http://www.freescale.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
LVDS_TX0+	LVDS channel 0 differential data output positive line	88	O	LVDS0_TX0_P	-
LVDS_TX0-	LVDS channel 0 differential data output negative line	90	O	LVDS0_TX0_N	-
LVDS_TX1+	LVDS channel 1 differential data output positive line	92	O	LVDS0_TX1_P	-
LVDS_TX1-	LVDS channel 1 differential data output negative line	94	O	LVDS0_TX1_N	-
LVDS_TX2+	LVDS channel 2 differential data output positive line	93	O	LVDS0_TX2_P	-
LVDS_TX2-	LVDS channel 2 differential data output negative line	95	O	LVDS0_TX2_N	-
LVDS_TX3+	LVDS channel 3 differential data output positive line	96	O	LVDS0_TX3_P	-
LVDS_TX3-	LVDS channel 3 differential data output negative line	98	O	LVDS0_TX3_N	-
LVDS_CLK+	LVDS differential clock output positive line	97	O	LVDS0_CLK_P	-
LVDS_CLK-	LVDS differential clock output negative line	99	O	LVDS0_CLK_N	-

Table 23: LVDS 1 Interface

3.12.3 LVDS channel 2

The DHCOM-X connector provides a second LVDS channel. By using both channels it is possible to support dual-channel LVDS displays. For LVDS feature description please have a look at 3.12.2.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
LVDS2_TX0+	LVDS 2 differential data lane 0 positive	60	O	LVDS1_TX0_P	-
LVDS2_TX0-	LVDS 2 differential data lane 0 negative	62	O	LVDS1_TX0_N	-
LVDS2_TX1+	LVDS 2 differential data lane 1 positive	64	O	LVDS1_TX1_P	-
LVDS2_TX1-	LVDS 2 differential data lane 1 negative	66	O	LVDS1_TX1_N	-
LVDS2_TX2+	LVDS 2 differential data lane 2 positive	59	O	LVDS1_TX2_P	-
LVDS2_TX2-	LVDS 2 differential data lane 2 negative	61	O	LVDS1_TX2_N	-
LVDS2_TX3+	LVDS 2 differential data lane 3 positive	63	O	LVDS1_TX3_P	-
LVDS2_TX3-	LVDS 2 differential data lane 3 negative	65	O	LVDS1_TX3_N	-
LVDS2_CLK+	LVDS 2 differential clock positive	55	O	LVDS1_CLK_P	-
LVDS2_CLK-	LVDS 2 differential clock negative	57	O	LVDS1_CLK_N	-

Table 24: LVDS 2 Interface

3.12.4 HDMI

The DHCOM-X connector provides a High Definition Multimedia interface with the following characteristics:

- HDMI 1.4a compliant
- DVI 1.0 compliant
- Up to 1080p @120Hz
- IEC60958, IEC61937 audio standard compliant

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
HDMI_D0+	HDMI differential data lane 0 positive	48	O	HDMI_D0P	HDMI	-
HDMI_D0-	HDMI differential data lane 0 negative	50	O	HDMI_D0M	HDMI	-
HDMI_D1+	HDMI differential data lane 1 positive	52	O	HDMI_D1P	HDMI	-
HDMI_D1-	HDMI differential data lane 1 negative	54	O	HDMI_D1M	HDMI	-
HDMI_D2+	HDMI or DP differential data lane 2 positive	47	O	HDMI_D2P	HDMI	-
HDMI_D2-	HDMI or DP differential data lane 2 negative	49	O	HDMI_D2M	HDMI	-
HDMI_CLK+	HDMI differential clock positive	43	O	HDMI_CLKP	HDMI	-
HDMI_CLK-	HDMI differential clock negative	45	O	HDMI_CLKM	HDMI	-
HDMI_HPD	HDMI or DP hot plug detect	56	I	HDMI_HPD	2V5	-

Table 25: HDMI Interface

3.13 PWM

The DHCM-iMX6-01D2 module enables the connection to Pulse Width Modulation (PWM) output.

More precise information about this is available in the i.MX6 Reference Manual:

http://www.freescale.com/

Note: DHCOM PWM uses the PWM1 instance of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
GPIO_PWM	PWM channel (only if LCD contrast is not used)	100	O	SD1_DAT3	-

Table 26: PWM Interface

3.14 SD/MMC/SDIO controller

The i.MX6 processor has a SD/MMC/SDIO card host controller integrated. Two controllers are used on the module, one for access to the on-board microSD card, the other as a SD/MMC/SDIO interface to the SODIMM-200 socket.

Main characteristics:

- Compatible with the MMC System Specification version 4.2/4.3/4.4
- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the SDIO Card Specification version 3.0
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit MMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- …

3.14.1 On-board microSD socket

Note: DHCOM microSD socket uses the SD3 instance of the i.MX6.

Signal name	Description	uSD socket pin number	IO Type	CPU ball name
SD_CLK	SD/SDIO/MMC bus clock	5	O	SD3_CLK
SD_CMD	SD/SDIO/MMC command line	3	IO	SD3_CMD
SD_DETECT	SD/SDIO/MMC card detection (LOW when card inserted)	G3	I	SD3_RST
SD_D0	SD/SDIO/MMC data line	7	IO	SD3_DAT0
SD_D1	SD/SDIO/MMC data line	8	IO	SD3_DAT1
SD_D2	SD/SDIO/MMC data line	1	IO	SD3_DAT2
SD_D3	SD/SDIO/MMC data line	2	IO	SD3_DAT3

Table 27: On-board microSD card socket

3.14.2 SD/MMC/SDIO interface

Note: DHCOM SD interface uses the SD2 instance of the i.MX6.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	SD2_CLK	-
SD_CMD	SD/SDIO/MMC command line	104	IO	SD2_CMD	-
SD_DETECT	SD/SDIO/MMC card detection(active high)	105	I	NANDF_CS3	PD
SD_D0	SD/SDIO/MMC data line	106	IO	SD2_DAT0	-

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SD_D1	SD/SDIO/MMC data line	107	IO	SD2_DAT1	-
SD_D2	SD/SDIO/MMC data line	108	IO	SD2_DAT2	-
SD_D3	SD/SDIO/MMC data line	109	IO	SD2_DAT3	-

Table 28: SD/MMC/SDIO Interface

3.15 GPIOs

The DHCM-iMX6-01D2 module provides several GPIO pins on the SODIMM-200 socket.

Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHCOM standard.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Out of reset state	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	IO	KEY_COL0	In / 100k PU	PU
GPIO _A	General Purpose I/O	154	IO	GPIO_2	In / 100k PU	-
GPIO _B	General Purpose I/O	156	IO	GPIO_4	In / 100k PU	-
GPIO _C	General Purpose I/O	162	IO	GPIO_5	In / 100k PU	-
GPIO _D	General Purpose I/O	163	IO	CSI0_DAT17	In / 100k PU	-
GPIO _E	General Purpose I/O	164	IO	GPIO_19	In / 100k PU	-
GPIO _F	General Purpose I/O	165	IO	DI0_PIN4	In / 100k PU	-
GPIO _G	General Purpose I/O	167	IO	EIM_D27	In / 100k PU	-
GPIO _H	General Purpose I/O	173	IO	KEY_ROW0	In / 100k PU	-
GPIO _I	General Purpose I/O	175	IO	KEY_COL1	In / 100k PU	-
VIO_OUT	Voltage for external Level-Shifter	152	PWR_O	-	-	-
GPIO_J (or CIF_HSYNC)	General Purpose I/O	74	IO	NANDF_CS1	In / 100k PU	-
GPIO_K (or CIF_PCLK)	General Purpose I/O	72	IO	NANDF_CS2	In / 100k PU	-
GPIO_L (or CIF_MCLK)	General Purpose I/O	70	IO	KEY_ROW1	In / 100k PU	-
GPIO_M (or CIF_VSYNC)	General Purpose I/O	68	IO	SD3_DAT5	In / 100k PU	-
GPIO_N (or CIF_D9)	General Purpose I/O	66	IO	SD3_DAT4	In / 100k PU	-
GPIO_O (or CIF_D8)	General Purpose I/O	64	IO	CSI0_VSYNC	In / 100k PU	-
GPIO_P (or CIF_D7)	General Purpose I/O	62	IO	GPIO_18	In / 100k PU	-
GPIO_Q (or CIF_D6)	General Purpose I/O	60	IO	SD1_CMD	In / 100k PU	-
GPIO_R (or CIF_D5)	General Purpose I/O	58	IO	SD1_DAT0	In / 100k PU	-
GPIO_S (or CIF_D4)	General Purpose I/O	56	IO	SD1_DAT1	In / 100k PU	-
GPIO_T (or CIF_D3)	General Purpose I/O	54	IO	SD1_DAT2	In / 100k PU	-
GPIO_U (or CIF_D2)	General Purpose I/O	52	IO	SD1_CLK	In / 100k PU	-
GPIO_V (or CIF_D1)	General Purpose I/O	50	IO	CSI0_PIXCLK	In / 100k PU	-
GPIO_W (or CIF_D0)	General Purpose I/O	48	IO	CSI0_MCLK	In / 100k PU	-
Vcam_OUT	Voltage for external Level-Shifter	102	PWR_O	-	-	-

Table 29: GPIO pin assignment

Note: The GPIOs of the i.MX6 can only drive at a maximum of roughly 2mA (depends on the pad drive strength). Where a greater current is required, an additional driver must be provided on the carrier board. The minimum and maximum logic level can be obtained from the data sheet of the i.MX6.

http://www.freescale.com/

3.16 RGMII (Gbit Ethernet)

The DHCOM-X connector provides an RGMII interface. This is the standard interface between Ethernet MAC and PHY for Gbit Ethernet.

Note: The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to Chip internal bus throughput limitation. The actual measured performance in an optimized environment is up to 400 Mbps. See erratum ERR004512 in the device silicon errata document.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
RGMII_TXCLK	RGMII transmit clock, 125 MHz digital	2	O	RGMII_TXC	Vrgmii	-
RGMII_TXD0	RGMII transmit data 0	4	O	RGMII_TD0	Vrgmii	-
RGMII_TXD1	RGMII transmit data 1	6	O	RGMII_TD1	Vrgmii	-
RGMII_TXD2	RGMII transmit data 2	8	O	RGMII_TD2	Vrgmii	-
RGMII_TXD3	RGMII transmit data 3	10	O	RGMII_TD3	Vrgmii	-
RGMII_TX_CTL	RGMII transmit enable	12	O	RGMII_TX_CTL	Vrgmii	-
RGMII_RXCLK	RGMII receive clock, 125 MHz digital	1	I	RGMII_RXC	Vrgmii	-
RGMII_RXD0	RGMII received data 0	3	I	RGMII_RD0	Vrgmii	-
RGMII_RXD1	RGMII received data 1	5	I	RGMII_RD1	Vrgmii	-
RGMII_RXD2	RGMII received data 2	7	I	RGMII_RD2	Vrgmii	-
RGMII_RXD3	RGMII received data 3	9	I	RGMII_RD3	Vrgmii	-
RGMII_RX_CTL	RGMII receive data valid	11	I	RGMII_RX_CTL	Vrgmii	-
RGMII_MDC	Management data clock	14	O	ENET_MDC	Vrgmii	-
RGMII_MDIO	Management data	13	IO	ENET_MDIO	Vrgmii	-
RGMII_REFCLK	MAC reference clock input (125MHz)	16	I	ENET_REF_CLK	Vrgmii	-
RGMII_RST	PHY reset	15	O	EIM_D29	Vrgmii	-
RGMII_INT	PHY interrupt (active low)	18	I	GPIO_0	3V3	PU
RGMII_WOL_INT	PHY Wake-on-LAN interrupt (active low)	17	I	EIM_D26	3V3	PU
VCC_RGMII_OUT	2,5V Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	-	Vrgmii	-

Table 30: RGMII Interface

3.17 Sata

The DHCOM-X connector provides a serial ATA (SATA, also S-ATA/Serial Advanced Technology Attachment) interface with the following characteristics:

- Compliant with the following specifications:
  - Serial ATA 3.0
  - AHCI Revision 1.3
  - AMBA 2.0 from ARM
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
SATA_TX+	SATA transmit data positive	24	O	SATA_TXP	Sata	-

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
SATA_TX-	SATA transmit data negative	26	O	SATA_TXM	Sata	-
SATA_RX+	SATA receive data positive	21	I	SATA_RXP	Sata	-
SATA_RX-	SATA receive data negative	23	I	SATA_RXM	Sata	-

Table 31: Sata Interface

3.18 PCIe

The DHCOM-X connector provides a "Peripheral Component Interconnect Express" interface with the following characteristics:

- 5Gb/s PCIe Gen 2 supported
- 2.5Gb/s PCIe Gen 1.1 supported

Note: PCIe reference clock solution which provided by CLK1_N/P of i.MX6 chip can't pass PCIe Gen2 compliance test (This note belongs to Hardware 493-300 (see 3.2 Hardware coding) and will be fixed in next generation).

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
PCIE_RX+	PCIe receive data positive	27	I	PCIE_RXP	PCIe	-
PCIE_RX-	PCIe receive data negative	29	I	PCIE_RXM	PCIe	-
PCIE_TX+	PCIe transmit data positive	31	O	PCIE_TXP	PCIe	-
PCIE_TX-	PCIe transmit data negative	33	O	PCIE_TXM	PCIe	-
PCIE_REFCLK+	PCIe 100MHz reference clock output positive	30	O	CLK1_P	PCIe	-
PCIE_REFCLK-	PCIe 100MHz reference clock output negative	32	O	CLK1_N	PCIe	-
PCIE_WAKE	PCIe wake signal (active low)	34	I	CSI0_DATA_EN	3V3	PU

Table 32: PCIe Interface

3.19 MIPI CSI-2

The DHCOM-X connector provides a Camera Serial Interface (CSI-2 spec. from MIPI Alliance) with the following characteristics:

- Support from 80 Mbps up to 1 Gbps speed per data lane
- Two data lanes with maximum transfer rate of 2Gbps
- D-PHY serves as physical layer for MIPI CSI-2 interface

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Voltage level	Not used
CSI_D0+	CSI received data 0 positive	38	I	CSI_D0P	CSI	-
CSI_D0-	CSI received data 0 negative	40	I	CSI_D0M	CSI	-
CSI_D1+	CSI received data 1 positive	42	I	CSI_D1P	CSI	-
CSI_D1-	CSI received data 1 negative	44	I	CSI_D1M	CSI	-
CSI_CLK+	CSI reference clock positive	37	I	CSI_CLK0P	CSI	-
CSI_CLK-	CSI reference clock negative	39	I	CSI_CLK0M	CSI	-

Table 33: MIPI CSI-2 Interface

4 Plugs and connections

Additionally to the SODIMM-200 connector, the DHCM-iMX6-01D2 module is equipped with Molex high speed connector, a 10pin FFC JTAG connector and a separate microSD card socket.

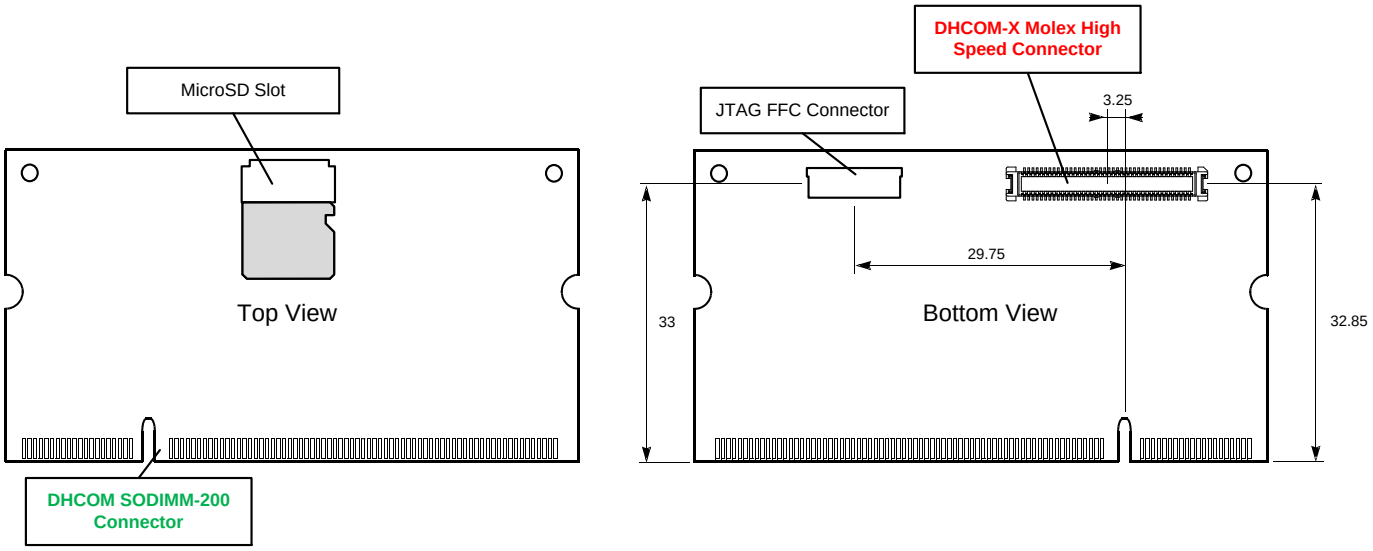


Figure 7: Position of the plugs and connections

4.1 SODIMM-200

Pin number	Pin name	Power domain
1	*Reserved*	VDDA
3	*Reserved*	VDDA
5	I2S_RXD	VIO
7	*Reserved*	VDDA
9	*Reserved*	VDDA
11	I2S_TXFS	VIO
13	I2S_TXC	VIO
15	I2S_TXD	VIO
17	GND1	Vin
19	GND2	Vin
21	RESET_IN	VIO
23	UART3_RX	VIO
25	UART3_TX	VIO
27	CAN_TX	VIO
29	CAN_RX	VIO
31	UART2_CTS	VIO
33	UART2_RTS	VIO
35	UART2_RX	VIO
37	UART2_TX	VIO
39	VCC_IN2	Vin
41	VCC_IN4	Vin
43	GND3	Vin
45	GND4	Vin

Pin number	Pin name	Power domain
2	*Reserved*	VDDA
4	*Reserved*	VDDA
6	*Reserved*	VDDA
8	Analog Input 0	VDDA
10	VDDA (Audio Supply VCC)	VDDA
12	TSPX	VDDA
14	TSMX	VDDA
16	TSMY	VDDA
18	TSPY	VDDA
20	RESET_OUT	VIO
22	UART1_DTR	VIO
24	UART1_CTS	VIO
26	UART1_RTS	VIO
28	UART1_DSR	VIO
30	UART1_DCD	VIO
32	UART1_RX	VIO
34	UART1_TX	VIO
36	UART1_RI	VIO
38	VCC_IN1	Vin
40	VCC_IN3	Vin
42	VCC_IN5	Vin
44	VCC_IN6	Vin
46	Vdisp_OUT	Vdisp

Pin number	Pin name	Power domain
47	GND5	Vin
49	LC_R2	Vdisp
51	LC_R3	Vdisp
53	LC_R4	Vdisp
55	LC_R5	Vdisp
57	LC_R6	Vdisp
59	LC_R7	Vdisp
61	LC_G2	Vdisp
63	LC_G3	Vdisp
65	LC_G4	Vdisp
67	LC_G5	Vdisp
69	LC_G6	Vdisp
71	LC_G7	Vdisp
73	LC_B2	Vdisp
75	LC_B3	Vdisp
77	LC_B4	Vdisp
79	LC_B5	Vdisp
81	LC_B6	Vdisp
83	LC_B7	Vdisp
85	LC_EN	Vdisp
87	LC_VSYNC	Vdisp
89	LC_HSYNC	Vdisp
91	LC_PCLK	Vdisp
93	LVDS_TX2+	LVDS
95	LVDS_TX2-	LVDS
97	LVDS_CLK+	LVDS
99	LVDS_CLK-	LVDS
101	GND6	Vin
103	SD_CLK	VIO
105	SD_DETECT	VIO
107	SD_D1	VIO
109	SD_D3	VIO
111	GND7	Vin
113	A0	Vsysbus
115	A1	Vsysbus
117	A2	Vsysbus
119	A3	Vsysbus
121	A4	Vsysbus
123	A5	Vsysbus
125	A6	Vsysbus
127	A7	Vsysbus
129	CS_B	Vsysbus
131	*Reserved*	Vsysbus
133	WE	Vsysbus
135	D0	Vsysbus
137	D1	Vsysbus
139	D2	Vsysbus
141	D3	Vsysbus
143	D4	Vsysbus

Pin number	Pin name	Power domain
48	GPIO_W (or CIF_D0)	Vcam
50	GPIO_V (or CIF_D1)	Vcam
52	GPIO_U (or CIF_D2)	Vcam
54	GPIO_T (or CIF_D3)	Vcam
56	GPIO_S (or CIF_D4)	Vcam
58	GPIO_R (or CIF_D5)	Vcam
60	GPIO_Q (or CIF_D6)	Vcam
62	GPIO_P (or CIF_D7)	Vcam
64	GPIO_O (or CIF_D8)	Vcam
66	GPIO_N (or CIF_D9)	Vcam
68	GPIO_M (or CIF_VSYNC)	Vcam
70	GPIO_L (or CIF_MCLK)	Vcam
72	GPIO_K (or CIF_PCLK)	Vcam
74	GPIO_J (or CIF_HSYNC)	Vcam
76	LC_R0	Vdisp
78	LC_R1	Vdisp
80	LC_G0	Vdisp
82	LC_G1	Vdisp
84	LC_B0	Vdisp
86	LC_B1	Vdisp
88	LVDS_TX0+	LVDS
90	LVDS_TX0-	LVDS
92	LVDS_TX1+	LVDS
94	LVDS_TX1-	LVDS
96	LVDS_TX3+	LVDS
98	LVDS_TX3-	LVDS
100	GPIO_PWM	VIO
102	Vcam_OUT	Vcam
104	SD_CMD	VIO
106	SD_D0	VIO
108	SD_D2	VIO
110	Vsysbus_OUT	Vsysbus
112	A8	Vsysbus
114	A9	Vsysbus
116	A10	Vsysbus
118	A11	Vsysbus
120	A12	Vsysbus
122	A13	Vsysbus
124	A14	Vsysbus
126	A15	Vsysbus
128	CS_A	Vsysbus
130	*Reserved*	Vsysbus
132	*Reserved*	Vsysbus
134	OE	Vsysbus
136	D8	Vsysbus
138	D9	Vsysbus
140	D10	Vsysbus
142	D11	Vsysbus
144	D12	Vsysbus

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
145	D5	Vsysbus	146	D13	Vsysbus
147	D6	Vsysbus	148	D14	Vsysbus
149	D7	Vsysbus	150	D15	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO	152	VIO_OUT	VIO
153	GND8	Vin	154	GPIO_A	VIO
155	SPI2_CS0	VIO	156	GPIO_B	VIO
157	SPI2_CLK	VIO	158	I2C2_CLK	VIO
159	SPI2_MISO	VIO	160	I2C2_DATA	VIO
161	SPI2_MOSI	VIO	162	GPIO_C	VIO
163	GPIO_D	VIO	164	GPIO_E	VIO
165	GPIO_F	VIO	166	USB_OTG_VBUS	USB
167	GPIO_G	VIO	168	USB_OTG_ID	USB
169	*Reserved*	USB	170	USB_OTG_D+	USB
171	*Reserved*	USB	172	USB_OTG_D-	USB
173	GPIO_H	VIO	174	USB_PWR_STAT	VIO
175	GPIO_I	VIO	176	USB_PWR_EN	VIO
177	SPI1_CS0	VIO	178	USB_HOST_D1+	USB
179	SPI1_CLK	VIO	180	USB_HOST_D1-	USB
181	SPI1_MISO	VIO	182	I2C1_CLK	VIO
183	SPI1_MOSI	VIO	184	I2C1_DATA	VIO
185	GND9	Vin	186	nETH1_LINK_LED	VIO
187	*Reserved*	VIO	188	nETH1_SPEED_LED	VIO
189	*Reserved*	VIO	190	ETH1_TXD-	Ethernet
191	*Reserved*	Ethernet	192	ETH1_TXD+	Ethernet
193	*Reserved*	Ethernet	194	ETH_VIO_SWITCHED	VIO
195	*Reserved*	Ethernet	196	ETH1_RXI-	Ethernet
197	*Reserved*	Ethernet	198	ETH1_RXI+	Ethernet
199	GND10	Vin	200	VCC_BAT	Vbat

Table 34: SODIMM-200 pin assignment

4.2 DHCOM-X

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
1	RGMII_RXCLK	Vrgmii	2	RGMII_TXCLK	Vrgmii
3	RGMII_RXD0	Vrgmii	4	RGMII_TXD0	Vrgmii
5	RGMII_RXD1	Vrgmii	6	RGMII_TXD1	Vrgmii
7	RGMII_RXD2	Vrgmii	8	RGMII_TXD2	Vrgmii
9	RGMII_RXD3	Vrgmii	10	RGMII_TXD3	Vrgmii
11	RGMII_RX_CTL	Vrgmii	12	RGMII_TX_CTL	Vrgmii
13	RGMII_MDIO	Vrgmii	14	RGMII_MDC	Vrgmii
15	RGMII_RST	Vrgmii	16	RGMII_REFCLK	Vrgmii
17	RGMII_WOL_INT	3V3	18	RGMII_INT	3V3
19	GND	Vin	20	VCC_RGMII_OUT	Vrgmii
21	SATA_RX+	Sata	22	GND	Vin
23	SATA_RX-	Sata	24	SATA_TX+	Sata
25	GND	Vin	26	SATA_TX-	Sata
27	PCIE_RX+	PCIe	28	GND	Vin
29	PCIE_RX-	PCIe	30	PCIE_REFCLK+	PCIe
31	PCIE_TX+	PCIe	32	PCIE_REFCLK-	PCIe

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
33	PCIE_TX-	PCIe	34	PCIE_WAKE	3V3
35	GND	Vin	36	GND	Vin
37	CSI_CLK+	CSI	38	CSI_D0+	CSI
39	CSI_CLK-	CSI	40	CSI_D0-	CSI
41	GND	Vin	42	CSI_D1+	CSI
43	HDMI_CLK+	HDMI	44	CSI_D1-	CSI
45	HDMI_CLK-	HDMI	46	GND	Vin
47	HDMI_D2+	HDMI	48	HDMI_D0+	HDMI
49	HDMI_D2-	HDMI	50	HDMI_D0-	HDMI
51	*Reserved*	2V5	52	HDMI_D1+	HDMI
53	GND	Vin	54	HDMI_D1-	HDMI
55	LVDS2_CLK+	LVDS	56	HDMI_HPD	2V5
57	LVDS2_CLK-	LVDS	58	GND	Vin
59	LVDS2_TX2+	LVDS	60	LVDS2_TX0+	LVDS
61	LVDS2_TX2-	LVDS	62	LVDS2_TX0-	LVDS
63	LVDS2_TX3+	LVDS	64	LVDS2_TX1+	LVDS
65	LVDS2_TX3-	LVDS	66	LVDS2_TX1-	LVDS
67	GND	Vin	68	GND	Vin
69	*reserved*		70	*reserved*	
71	*reserved*		72	*reserved*	
73	*reserved*		74	*reserved*	
75	*reserved*		76	*reserved*	
77	*reserved*		78	*reserved*	
79	VCC_IN7	Vin	80	VCC_IN8	Vin

Table 35: DHCOM-X (Molex High Speed Connector)

4.3 JTAG

Pin number	Pin name
1	+3V3 Output
2	GND
3	JTAG_TMS
4	#JTAG_TRST
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	*Reserved*
10	*Reserved*

Table 36: JTAG interface pin assignment

5 Technical specifications

5.1 Operating conditions – Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT	3.2		5.5	V
VCC_{ripple} (Vin)	VCC ripple peak-to-peak		50	100	mV
V_{bat}	Battery voltage INPUT	1.3		5.5	V
V_{sysbus}	System bus voltage OUTPUT		3.3		V
$I_{Vsysbus}$	Vsysbus current			20	mA
V_{disp}	Display voltage OUTPUT		3.3		V
I_{Vdisp}	Vdisp current			20	mA
V_{cam}	Camera voltage OUTPUT		3.3		V
I_{Vcam}	Vcam current			20	mA
V_{IO}	I/O voltage OUTPUT		3.3		V
I_{VIO}	VIO current			20	mA
$V_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
$I_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED current			60	mA
$V_{VCC\_RGMII\_OUT}$	Supply voltage output for external PHY IO voltage		2.5		V
$I_{VCC\_RGMII\_OUT}$	VCC_RGMII_OUT current			100	mA
I_{Solo}	Solo operating current (without V*_OUT pins, VCC = 3.3V)		370	760	mA
P_{Solo} (Power)	Solo core module power consumption		1,2	2,5	W
$I_{DualLite}$	DualLite operating current (without V*_OUT pins, VCC = 3.3V)		450	1060	mA
$P_{DualLite}$ (Power)	DualLite core module power consumption		1,5	3,5	W
I_{Quad}	Quad operating current (without V*_OUT pins, VCC = 3.3V)		910	1670	mA
P_{Quad} (Power)	Quad core module power consumption		3	5,5	W
IVbat	Vbat input current			5	mA
IVbat_Stby	Vbat Standby input current		800	1000	nA
VIH_3V3	Digital input high voltage	2.0	3.3		V
VIL_3V3	Digital input low voltage		0	0.8	V

Table 37: DC operating conditions

5.2 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
RESET_IN	System Reset input assertion time (active low)	10			ms
RESET_OUT	System Reset output assertion time (active low)	10			ms

Table 38: Reset Timings

5.3 Dimensions

Notes:

- Figure 8 shows an example with 5,2mm SODIMM-200 socket height.
- Figure 8 only fits with Solo or DualLite core module variant. For Dual and Quad please have a look at the cooling concept.
- Figure 8 doesn't consider DHCOM-X (Molex High Speed Connector) socket.

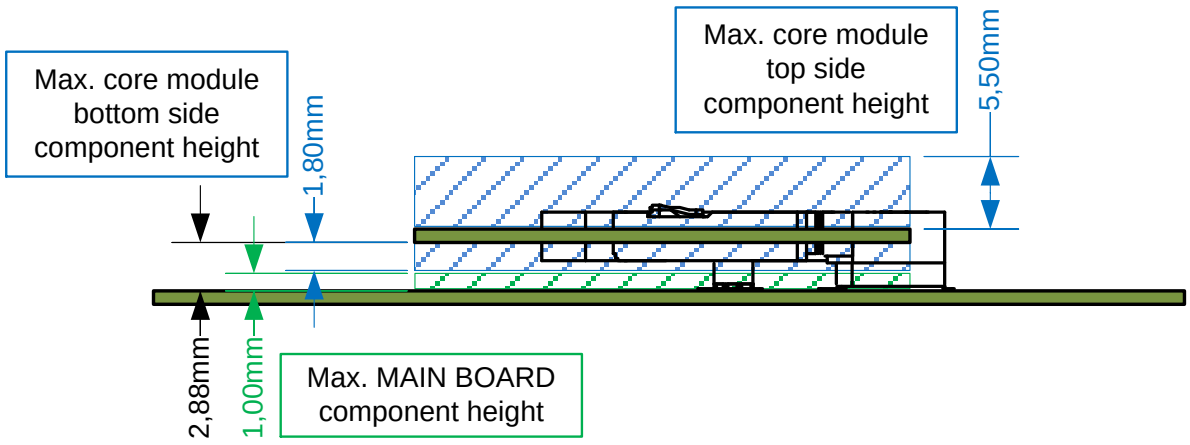
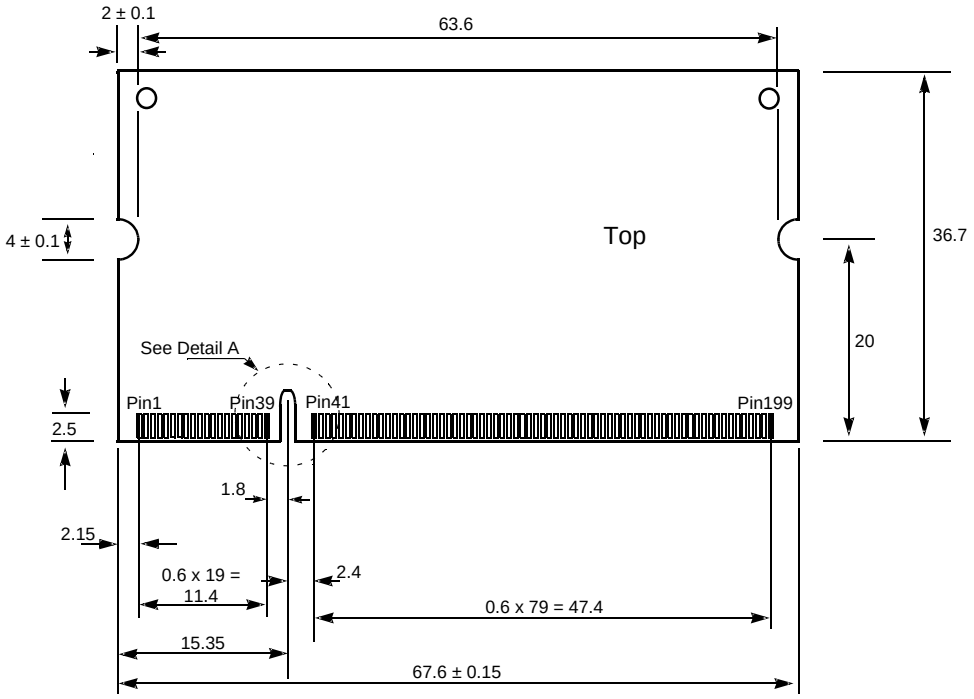
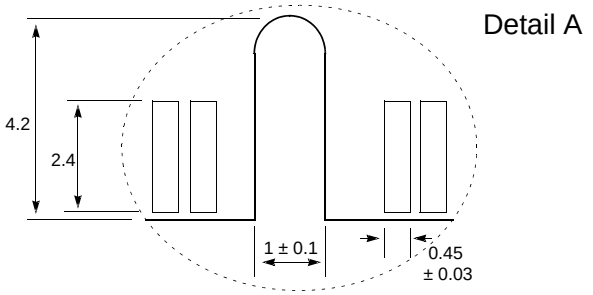


Figure 8: Maximum component heights





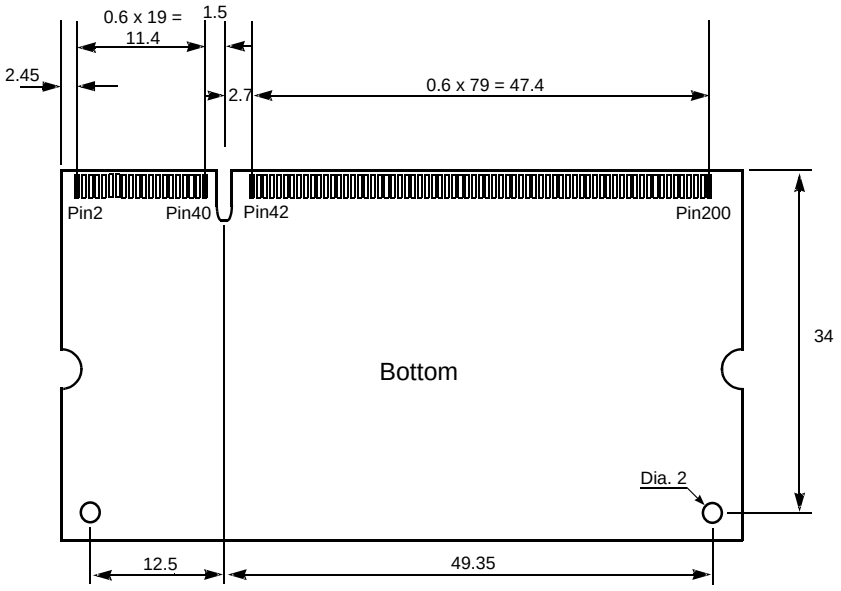


Figure 9: Dimensions of the module

5.4 Mechanical system

Several suggestions are given for the plugs, sockets and cables in the following subsections.

5.4.1 SODIMM-200 socket

The DHCM-iMX6-01D2 module is designed for operation in a standard 2.5V (DDR) SODIMM-200 memory socket.

DHCOM-X **note:** DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector.

The following sockets have been successfully tested with the module:

Manufacturer	Description	Article number
Nexus Components http://www.nexus-de.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	DMD-200-RSE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	1473005-1
Nexus Components http://www.nexus-de.com/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	DMD-200-RPE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	1612618-1

Table 39: SODIMM-200 sockets

5.4.2 DHCOM-X (Molex High Speed Connector)

A Molex (http://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector. DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

SODIMM-200 socket height	Description	Article number
5.2mm	0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits	Molex 53748-0808
9.2mm	Not available	Not available

Table 40: DHCOM-X (Molex High Speed Connector)

5.4.3 JTAG FFC cable

Manufacturer	Description	Article number
Würth Elektronik http://www.we-online.com	▪ 0.50 mm flat flexible cable Type 1 WR-FPC	687 610 050 002
Molex http://www.molex.com/	▪ 0.50mm flat flexible cable Type A	982660097

Table 41: FFC Cable

5.5 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C

Table 42: Temperature range

6 RoHS conformance

This device has been manufactured RoHS II-compliant.