DHCOR I.MX6UL(L)

User Manual

DH electronics GmbH | Am Anger 8 | 83346 Bergen | Germany

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Changes

Version	Date	Changes	Name
R01	2019-04-05	First draft	AG
R02	2019-10-17	Added chapter "JTAG" Adjust chapter "Boot Mode" Adjust chapter "WiFi / Bluetooth" Added chapter "UART for ..." Adjust chapter "Reset" Adjust chapter "SPI Flash" Added chapter "Assembly instructions" Added chapter "Hardware design checklist" Added chapter "eMMC connection" Added thermal example	AG
R02	2019-12-13	Released	HH
R02	2020-03-31	Updated Bluetooth Version to 5.1	MAD

Index of Contents

1 Introduction 6
1.1 Hardware 6
1.2 Software 6
1.3 Main characteristics 6
1.4 CPU differences 7
1.5 Further technical information 7
1.5.1 NXP i.MX6ULL processor 7
1.5.2 PMIC 7
1.5.3 WiFi/BT 7
2 Hardware overview 8
2.1 Block diagram 8
2.2 Pin assignment 8
3 Power supply and reset 15
3.1 Power supply 15
3.2 Power sequencing 15
4 Reset 15
5 Hardware and DDR3 coding 16
6 JTAG 17
7 SPI Flash 18
8 I²C™ 19
9 Boot Mode 20
10 UART for bootloader and Linux console 21
11 WiFi / Bluetooth 22
12 eMMC connection 23
13 Technical specifications 27
13.1 Operating conditions – Absolute maximum ratings 27

13.2 Reset Timings 27
13.3 Temperature range 27
14 Mechanical specifications 29
14.1 Dimensions 29
15 Assembly instructions 30
15.1 Moisture sensitivity and shelf life 30
15.2 Coplanarity 30
15.3 Solder pastes 30
15.4 Reflow Process 30
16 Tape and reel packaging 32
17 Hardware design checklist 32
18 RoHS conformance 33

Abbreviations

- AIN = Analog input
- AINOUT = Analog input/output
- I = Input
- IO = Input/output
- MBC = Must be connected
- O = Output
- PD = Pull-Down
- PU = Pull-Up
- PWR_I = Power input
- PWR_O = Power output
- TBD = To be defined

1 Introduction

1.1 Hardware

The DHCOR-iMX6UL(L)-01LG module is a computer module on a circuit board with the size of 29 mm by 29 mm which can be soldered onto other circuit boards. The CPU is designed by NXP and is based on a Cortex-A7 processor. It is clocked up to 900 MHz and is equipped with up to 1 GByte DDR3-Memory and 16 GByte eMMC flash. Numerous interfaces are also available for communicating with the outside world, which are required in embedded systems.

1.2 Software

Currently, the DHCOR-iMX6UL(L)-01LG module is available with the Embedded Linux operating system.

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.

1.3 Main characteristics

- Cortex-A7 NXP i.MX6UL(L) up to 900 MHz
- Absolute power efficient and cost optimized application processor
- Crypto Engine, Secure Boot
- 2 MByte SPI boot flash
- 128 - 1024 MByte DDR3 memory
- MMC 4.5 / SD 3.0 / SDIO Port (1-/2-/4-bit)
- eMMC 4.4 / 4.41
- QuadSPI interface
- NAND 8 bit Raw MLC / SLC
- Address / data 16 bit bus interface
- Ethernet 10 / 100 Mbit, IEEE 1588: 2x
- LC display controller, 24 bit colors, max. 1366x768 pixels
- CSI parallel camera interface, 8 bit / pixel data format
- On-board touch controller for 4-wire resistive touch screens
- USB 2.0 OTG 1 high-speed
- USB 2.0 OTG 2 high-speed
- UART up to 5.0 Mbit/s: 8x

- CAN V2.0B, 1 Mbit/s: 2x
- SPI max. 52 Mbps: 4x
- I2C™ max. 400 kbit: 4x
- I²S / SAI Audio interface: 3x
- Real-time clock RTC
- PWM / Timer: 8x 16 bit PWM / 4x 32 bit Timer
- 95 GPIOs
- JTAG debug interface
- Industrial temperature range (-40°C to +85°C)
- WiFi: IEEE802.11b/g/n W-LAN
- Bluetooth: Bluetooth® v4.1 (BR/EDR/BLE)

1.4 CPU differences

For more information and differences between i.MX6ULL and i.MX6UltraLite processor, we refer you to the web-site of NXP https://www.nxp.com/

1.5 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

1.5.1 NXP i.MX6ULL processor

Data sheets and technical documents can be found at https://www.nxp.com/

1.5.2 PMIC

Data sheets and technical documents can be found at https://www.dialog-semiconductor.com/

1.5.3 WiFi/BT

Data sheets and technical documents can be found at https://wireless.murata.com

2 Hardware overview

2.1 Block diagram

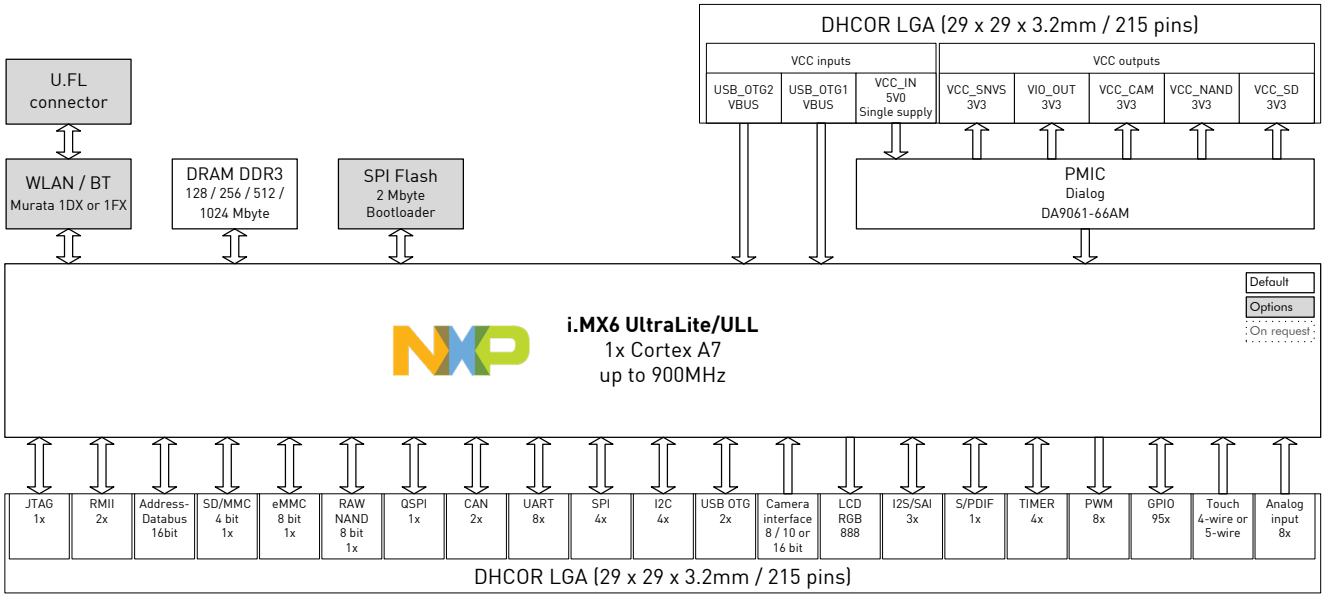

Figure 1: DHCOR-iMX6UL(L)-01LG block diagram

2.2 Pin assignment

The DHCOR-iMX6UL(L)-01LG comes with the i.MX6 CPU package of 14 x 14 mm.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec-tions on DHCOR	Pin not used
NAND_nREADY / QSPI_DAT0	NAND_READY_B	A2	GPIO	Input	NAND_READY_B	A3	-	Keeper
NAND_CLE / QSPI_DAT3	NAND_CLE	A3	GPIO	Input	NAND_CLE	A4	-	Keeper
NAND_DAT7 / SD2_DAT7	NAND_DATA07	A4	GPIO	Input	NAND_DATA07	A5	-	Keeper
NAND_DAT6 / SD2_DAT6	NAND_DATA06	A5	GPIO	Input	NAND_DATA06	A6	-	Keeper
NAND_DAT2 / SD2_DAT2	NAND_DATA02	A6	GPIO	Input	NAND_DATA02	A7	-	Keeper
NAND_DAT1 / SD2_DAT1	NAND_DATA01	A7	GPIO	Input	NAND_DATA01	B7	-	Keeper
CSI_MCLK	CSI_MCLK	A8	GPIO	Input	CSI_MCLK	F5	-	Keeper
CSI_DATA00	CSI_DATA00	A9	GPIO	Input	CSI_DATA00	E4	-	Keeper
CSI_DATA01	CSI_DATA01	A10	GPIO	Input	CSI_DATA01	E3	-	Keeper
VCC_CAM	VCC_CAM	A11	PWR	Output	-	-	-	-
VCC_SD	VCC_SD	A12	PWR	Output	-	-	-	-
VCC_NAND	VCC_NAND	A13	PWR	Output	-	-	-	-
VCC_NAND	VCC_NAND	A14	PWR	Output	-	-	-	-
VCC_SNVS	VDD_SNVS_IN_3V3	A15	PWR	Output	-	-	-	-
NC	Not connected	A16	-	-	-	-	-	-
NC	Not connected	A17	-	-	-	-	-	-
NC	Not connected	A18	-	-	-	-	-	-
NC	Not connected	A19	-	-	-	-	-	-
VIO_OUT	VCC_3V3	A20	PWR	Output	-	-	-	-

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
VIO_OUT	VCC_3V3	A21	PWR	Output	-	-	-	-
NAND_nRE / SD2_CLK	NAND_RE_B	B1	GPIO	Input	NAND_RE_B	D8	-	Keeper
NAND_nCE0 / QSPI_DAT1	NAND_CE0_B	B2	GPIO	Input	NAND_CE0_B	C5	-	Keeper
NAND_DAT4 / SD2_DAT4	NAND_DATA04	B3	GPIO	Input	NAND_DATA04	C6	-	Keeper
NAND_nWE / SD2_CMD	NAND_WE_B	B4	GPIO	Input	NAND_WE_B	C8	-	Keeper
NAND_ALE / SD2_nRST	NAND_ALE	B5	GPIO	Input	NAND_ALE	B4	-	Keeper
NAND_nCE1 / QSPI_DAT2	NAND_CE1_B	B6	GPIO	Input	NAND_CE1_B	B5	-	Keeper
NAND_DAT5 / SD_DAT5	NAND_DATA05	B7	GPIO	Input	NAND_DATA05	B6	-	Keeper
CSI_PIXCLK	CSI_PIXCLK	B8	GPIO	Input	CSI_PIXCLK	E5	-	Keeper
CSI_DATA02	CSI_DATA02	B9	GPIO	Input	CSI_DATA02	E2	-	Keeper
CSI_DATA03	CSI_DATA03	B10	GPIO	Input	CSI_DATA03	E1	-	Keeper
VCC_IN_5V	VCC_IN_5V	B11	PWR	Input	-	-	-	-
VCC_IN_5V	VCC_IN_5V	B12	PWR	Input	-	-	-	-
GND	GND	B13	PWR	-	-	-	-	-
GND	GND	B14	PWR	-	-	-	-	-
GND	GND	B15	PWR	-	-	-	-	-
GND	GND	B16	PWR	-	-	-	-	-
VCC_IN_5V	VCC_IN_5V	B17	PWR	Input	-	-	-	-
VCC_IN_5V	VCC_IN_5V	B18	PWR	Input	-	-	-	-
NC	Not connected	B19	-	-	-	-	-	-
VIO_OUT	VCC_3V3	B20	PWR	Output	-	-	-	-
VIO_OUT	VCC_3V3	B21	PWR	Output	-	-	-	-
NAND_nWP / QSPI_SCLK	NAND_WP_B	C1	GPIO	Input	NAND_WP_B	D5	-	Keeper
NAND_DAT3 / SD2_DAT3	NAND_DATA03	C2	GPIO	Input	NAND_DATA03	D6	-	Keeper
NAND_DAT0 / SD2_DAT0	NAND_DATA00	C3	GPIO	Input	NAND_DATA00	D7	-	Keeper
NC	Not connected	C4	-	-	-	-	-	-
CSI_DATA07 / ECSPI1_MISO	CSI_DATA07	C5	GPIO	Input	CSI_DATA07	D1	-	Keeper
CSI_DATA05 / ECSPI1_SS0	CSI_DATA05	C6	GPIO	Input	CSI_DATA05	D3	-	Keeper
CSI_HSYNC	CSI_HSYNC	C7	GPIO	Input	CSI_HSYNC	F3	-	Keeper
CSI_VSYNC	CSI_VSYNC	C8	GPIO	Input	CSI_VSYNC	F2	-	Keeper
CSI_DATA04 / ECSPI1_SCLK	CSI_DATA04	C9	GPIO	Input	CSI_DATA04	D4	-	Keeper
CSI_DATA06 / ECSPI1_MOSI	CSI_DATA06	C10	GPIO	Input	CSI_DATA06	D2	-	Keeper
VCC_IN_5V	VCC_IN_5V	C11	PWR	Input	-	-	-	-
VCC_IN_5V	VCC_IN_5V	C12	PWR	Input	-	-	-	-
GND	GND	C13	PWR	-	-	-	-	-
GND	GND	C14	PWR	-	-	-	-	-
GND	GND	C15	PWR	-	-	-	-	-
GND	GND	C16	PWR	-	-	-	-	-
VCC_IN_5V	VCC_IN_5V	C17	PWR	Input	-	-	-	-
VCC_IN_5V	VCC_IN_5V	C18	PWR	Input	-	-	-	-
NC	Not connected	C19	-	-	-	-	-	-
NC	Not connected	C20	-	-	-	-	-	-
NC	Not connected	C21	-	-	-	-	-	-
NAND_DQS / QSPI_nSS0	NAND_DQS	D1	GPIO	Input	NAND_DQS	E6	-	Keeper
BT_DEV_WAKE[1]	BT_DEV_WAKE	D2	-	-	-	-	-	-

[1] These pins are connected to the WiFi / Bluetooth module only. For more information see chapter 11 WiFi / Bluetooth.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
BT_HOST_WAKE[1]	BT_HOST_WAKE	D3	-	-	-	-	-	-
BT_REG_ON[1]	BT_REG_ON	E1	-	-	-	-	-	-
WL_HOST_WAKE[1]	WL_HOST_WAKE	E2	-	-	-	-	-	-
WL_REG_ON[1]	WL_REG_ON	E3	-	-	-	-	-	-
UART2_TX[2]	UART2_TX	F1	GPIO	Input	UART2_TX_DATA	J17	-	Keeper
UART2_RX[2]	UART2_RX	F2	GPIO	Input	UART2_RX_DATA	J16	-	Keeper
LPO_IN_32kHz[1]	Bluetooth?	F3	-	-	-	-	-	-
UART3_TX / UART2_CTS[2]	UART2_CTS	G1	GPIO	Input	UART3_TX_DATA	H17	-	Keeper
UART3_RX / UART2_RTS[2]	UART2_RTS	G2	GPIO	Input	UART3_RX_DATA	H16	-	Keeper
SD1_DATA0_LGA[3]	Not connected	G3	GPIO	Input	SD1_DATA0	B3	-	Keeper
SD1_DATA1_LGA[3]	Not connected	H1	GPIO	Input	SD1_DATA1	B2	-	Keeper
SD1_DATA2_LGA[3]	Not connected	H2	GPIO	Input	SD1_DATA2	B1	-	Keeper
SD1_DATA3_LGA[3]	Not connected	H3	GPIO	Input	SD1_DATA3	A2	-	Keeper
SD1_CMD_LGA[3]	Not connected	J1	GPIO	Input	SD1_CMD	C2	-	Keeper
SD1_CLK_LGA[3]	Not connected	J2	GPIO	Input	SD1_CLK	C1	-	Keeper
NC	Not connected	J3	-	-	-	-	-	-
JTAG_TDO / SAI2_SYNC	JTAG_TDO	K1	SJC	Output	JTAG_TDO	N15	-	Keeper
JTAG_TRST / SAI2_TXD	JTAG_TRST_B	K2	SJC	Input	JTAG_TRST_B	N14	-	47 kΩ PU
JTAG_TCK / SAI2_RXD	JTAG_TCK	K3	SJC	Input	JTAG_TCK	M14	-	47 kΩ PU
JTAG_TDI / SAI2_BCLK	JTAG_TDI	L1	SJC	Input	JTAG_TDI	N16	-	47 kΩ PU
JTAG_TMS / SAI2_MCLK	JTAG_TMS	L2	SJC	Input	JTAG_TMS	P14	-	47 kΩ PU
JTAG_MOD	JTAG_MOD	L3	SJC	Input	JTAG_MOD	P15	10k PD to GND	-
BT_GPIO_4[1]	BT_GPIO_4	M1	-	-	-	-	-	-
BT_GPIO_3[1]	BT_GPIO_3	M2	-	-	-	-	-	-
WL_GPIO_4[1]	WL_GPIO_4	M3	-	-	-	-	-	-
WL_GPIO_1[1]	WL_GPIO_1	N1	-	-	-	-	-	-
WL_GPIO_2[1]	WL_GPIO_2	N2	-	-	-	-	-	-
BT_I2S_DO[1]	BT_I2S_DO	N3	-	-	-	-	-	-
BT_GPIO_5[1]	BT_GPIO_5	P1	-	-	-	-	-	-
NC	Not connected	P2	-	-	-	-	-	-
NC	Not connected	P3	-	-	-	-	-	-
NC	Not connected	R1	-	-	-	-	-	-
NC	Not connected	R2	-	-	-	-	-	-
NC	Not connected	R3	-	-	-	-	-	-
NC	Not connected	T1	-	-	-	-	-	-
NC	Not connected	T2	-	-	-	-	-	-
NC	Not connected	T3	-	-	-	-	-	-
NC	Not connected	U1	-	-	-	-	-	-
NC	Not connected	U2	-	-	-	-	-	-
NC	Not connected	U3	-	-	-	-	-	-
NC	Not connected	V1	-	-	-	-	-	-

[2] UART2 is only available if WiFi is not mounted (module variant without option –WBT). Keep these pins open if WiFi is mounted.
[3] SD1 is only available if WiFi is not mounted (module variant without option –WBT).

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
NC	Not connected	V2	-	-	-	-	-	-
NC	Not connected	V3	-	-	-	-	-	-
POR_B (reset_out)	POR_B (reset_out)	D19	SRC	Input	POR_B	P8	1k PU to VCC_IN and connected to PMIC	100 kΩ PU
nONKEY[4]	nONKEY	D20	-	-	-	-	1k PU to VCC_IN and connected to PMIC	-
reset_in[4]	reset_in	D21	-	-	-	-	-	-
LCD_CLK	LCD_CLK[5]	E19	GPIO	Input	LCD_CLK	A8	10k PU to VIO_OUT or PD to GND	Keeper
LCD_DATA01	LCD_DATA01	E20	GPIO	Input	LCD_DATA01	B9	-	Keeper
LCD_DATA06	LCD_DATA06	E21	GPIO	Input	LCD_DATA06	A10	-	Keeper
LCD_DATA09	LCD_DATA09	F19	GPIO	Input	LCD_DATA09	A11	-	Keeper
LCD_DATA14	LCD_DATA14	F20	GPIO	Input	LCD_DATA14	A12	-	Keeper
LCD_DATA18	LCD_DATA18	F21	GPIO	Input	LCD_DATA18	A13	-	Keeper
LCD_DATA22 / ECSPI1_MOSI	ECSPI1_MOSI	G19	GPIO	Input	LCD_DATA22	A14	Connected to SPI flash	Keeper
LCD_EN	LCD_ENABLE[5]	G20	GPIO	Input	LCD_ENABLE	B8	10k PU to VIO_OUT or PD to GND	Keeper
LCD_DATA00	LCD_DATA00	G21	GPIO	Input	LCD_DATA00	B9	-	Keeper
LCD_DATA05	LCD_DATA05	H19	GPIO	Input	LCD_DATA05	B10	-	Keeper
LCD_DATA08	LCD_DATA08	H20	GPIO	Input	LCD_DATA08	B11	-	Keeper
LCD_DATA13	LCD_DATA13	H21	GPIO	Input	LCD_DATA13	B12	-	Keeper
LCD_DATA17	LCD_DATA17	J19	GPIO	Input	LCD_DATA17	B13	-	Keeper
LCD_DATA23 / ECSPI1_MISO	ECSPI1_MISO	J20	GPIO	Input	LCD_DATA23	B16	Connected to SPI flash	Keeper
LCD_DATA21 / ECSPI1_SS0	ECSPI1_SS0	J21	GPIO	Input	LCD_DATA21	B14	100k PU to VIO_OUT and con. to SPI flash	Keeper
LCD_VSYNC	LCD_VSYNC[6]	K19	GPIO	Input	LCD_VSYNC	C9	10k PU to VIO_OUT or PD to GND	Keeper
LCD_DATA04	LCD_DATA04	K20	GPIO	Input	LCD_DATA04	C10	-	Keeper
LCD_DATA12	LCD_DATA12	K21	GPIO	Input	LCD_DATA12	C12	-	Keeper
LCD_DATA16	LCD_DATA16	L19	GPIO	Input	LCD_DATA16	C13	-	Keeper
LCD_DATA20 / ECSPI1_SCLK	LCD_DATA20	L20	GPIO	Input	LCD_DATA20	C14	Connected to SPI flash	Keeper
LCD_HSYNC	LCD_HSYNC[6]	L21	GPIO	Input	LCD_HSYNC	D9	10k PU to VIO_OUT or PD to GND	Keeper

[4] nONKEY and Reset_in is connected to the PMIC only.
[5] LCD_CLK and LCD_ENABLE are also used for the Hardware and DDR3 coding, which means that either a pull-up or a pull-down resistor is connected to these pins. See chapter 5 Hardware and DDR3 coding for more information.
[6] LCD_VSYNC and LCD_HSYNC are also used to read out the size of the DDR3 memory of the DHCOR-iMX6UL(L)-01LG, which means that either a pull-up or a pull-down resistor is connected to these pins. See chapter 5 Hardware and DDR3 coding for more information.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
LCD_DATA03	LCD_DATA03	M19	GPIO	Input	LCD_DATA03	D10	-	Keeper
LCD_DATA07	LCD_DATA07	M20	GPIO	Input	LCD_DATA07	D11	-	Keeper
LCD_DATA11	LCD_DATA11	M21	GPIO	Input	LCD_DATA11	D12	-	Keeper
LCD_DATA15	LCD_DATA15	N19	GPIO	Input	LCD_DATA15	D13	-	Keeper
LCD_DATA19	LCD_DATA19	N20	GPIO	Input	LCD_DATA19	D14	-	Keeper
LCD_RESET / WDOG1	LCD_RESET	N21	GPIO	Input	LCD_RESET	E9	-	Keeper
LCD_DATA02	LCD_DATA02	P19	GPIO	Input	LCD_DATA02	E10	-	Keeper
LCD_DATA10	LCD_DATA10	P20	GPIO	Input	LCD_DATA10	E12	-	Keeper
ENET2_TX_DATA0	ENET2_TX_DATA0	P21	GPIO	Input	ENET2_TX_DATA0	A15	-	Keeper
ENET2_TX_DATA1 / ECSPI4_SCLK	ENET2_TX_DATA1	R19	GPIO	Input	ENET2_TX_DATA1	A16	-	Keeper
ENET2_TX_EN / ECSPI4_MOSI	ENET2_TX_EN	R20	GPIO	Input	ENET2_TX_EN	B15	-	Keeper
ENET2_RX_EN	ENET2_RX_EN	R21	GPIO	Input	ENET2_RX_EN	B17	-	Keeper
ENET2_RX_DATA1	ENET2_RX_DATA1	T19	GPIO	Input	ENET2_RX_DATA1	C16	-	Keeper
ENET2_RX_DATA0	ENET2_RX_DATA0	T20	GPIO	Input	ENET2_RX_DATA0	C17	-	Keeper
ENET2_RX_ER / ECSPI4_SS0	ENET2_RX_ER	T21	GPIO	Input	ENET2_RX_ER	D16	-	Keeper
ENET2_TX_CLK / ECSPI4_MISO	ENET2_TX_CLK	U19	GPIO	Input	ENET2_TX_CLK	D17	-	Keeper
ENET1_RX_ER	ENET1_RX_ER	U20	GPIO	Input	ENET1_RX_ER	D15	-	Keeper
ENET1_TX_DATA1	ENET1_TX_DATA1	U21	GPIO	Input	ENET1_TX_DATA1	E14	-	Keeper
ENET1_TX_DATA0	ENET1_TX_DATA0	V19	GPIO	Input	ENET1_TX_DATA0	E15	-	Keeper
ENET1_RX_EN	ENET1_RX_EN	V20	GPIO	Input	ENET1_RX_EN	G16	-	Keeper
ENET1_RX_DATA1	ENET1_RX_DATA1	V21	GPIO	Input	ENET1_RX_DATA1	F16	-	Keeper
NC	Not connected	W1	-	-	-	-	-	-
NC	Not connected	W2	-	-	-	-	-	-
NC	Not connected	W3	-	-	-	-	-	-
NC	Not connected	W4	-	-	-	-	-	-
NC	Not connected	W5	-	-	-	-	-	-
SNVS_TAMPER9 / GPIO5_IO9	GPIO5_IO9	W6	GPIO	Input	SNVS_TAMPER9	R6	-	Keeper / Not connected[8]
SNVS_TAMPER4 / GPIO5_IO4 / AUD_INT	GPIO5_IO4	W7	GPIO	Input	SNVS_TAMPER4	P9	-	Keeper / Not connected[8]
SNVS_TAMPER3 / GPIO5_IO3	GPIO5_IO3	W8	GPIO	Input	SNVS_TAMPER3	P10	-	Keeper / Not connected[8]
SNVS_TAMPER6 / GPIO5_IO6 / ENET2_INT	ENET2_INT	W9	GPIO	Input	SNVS_TAMPER6	N11	-	Keeper / Not connected[8]
UART5_TX / I2C2_SCL	I2C2_SCL	W10	GPIO	Input	UART5_TX_DATA	F17	-	Keeper
UART4_RX / I2C1_SDA	I2C1_SDA	W11	GPIO	Input	UART4_RX_DATA	G16	3k3 PU to VIO_OUT and connected to PMIC	Keeper
UART2_RTS / CAN2_RX	CAN2_RX	W12	GPIO	Input	UART2_RTS_B	H14	-	Keeper
UART1_RTS / SD1_CD	SD1_CD	W13	GPIO	Input	UART2_RTS_B	J14	-	Keeper

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
SPI_BOOT_FLASH_EN[7]	SPI_BOOT_FLASH_EN	W14	GPIO	Input	GPIO1_IO09	M15	10k PD to GND and con. to SPI flash	Keeper
GPIO1_IO07 / ENET_MDC / ADC1-IN7	ENET_MDC	W15	GPIO	Input	GPIO1_IO07	L16	-	Keeper
BOOT_MODE0	BOOT_MODE0	W16	GPIO	Input	BOOT_MODE0	T10	-	100 kΩ PD
GPIO1_IO06 / ENET_MDIO / ADC1_IN6	ENET_MDIO	W17	GPIO	Input	GPIO1_IO06	K17	-	Keeper
USB_OTG2_DN	USB_OTG2_DN	W18	Ana-log	-	USB_OTG2_DN	T13	-	-
ENET1_TX_CLK	ENET1_TX_CLK	W19	GPIO	Input	ENET1_TX_CLK	F14	-	Keeper
ENET1_TX_EN	ENET1_TX_EN	W20	GPIO	Input	ENET1_TX_EN	F14	-	Keeper
ENET1_RX_DATA0	ENET1_RX_DATA0	W21	GPIO	Input	ENET1_RX_DATA0	F16	-	Keeper
GND	GND	Y1	PWR	-	-	-	-	-
GND	GND	Y2	PWR	-	-	-	-	-
NC	Not connected	Y3	-	-	-	-	-	-
NC	Not connected	Y4	-	-	-	-	-	-
NC	Not connected	Y5	-	-	-	-	-	-
NC	Not connected	Y6	-	-	-	-	-	-
SNVS_TAMPER1 / GPIO5_IO1	GPIO5_IO1	Y7	GPIO	Input	SNVS_TAMPER1	R9	-	Keeper / Not connected[8]
SNVS_TAMPER0 / GPIO5_IO0	GPIO5_IO0	Y8	GPIO	Input	SNVS_TAMPER0	R10	-	Keeper / Not connected[8]
SNVS_TAMPER2 / GPIO5_IO2	GPIO5_IO2	Y9	GPIO	Input	SNVS_TAMPER2	P11	-	Keeper / Not connected[8]
UART5_RX / I2C2_SDA	I2C2_SDA	Y10	GPIO	Input	UART5_RX_DATA	J13	-	Keeper
UART3_RTS / CAN1_RX	CAN1_RX	Y11	GPIO	Input	UART3_RTS_B	H15	-	Keeper
UART2_CTS / CAN2_TX	CAN2_TX	Y12	GPIO	Input	UART2_CTS_B	J15	-	Keeper
UART1_TX	UART1_TX	Y13	GPIO	Input	UART1_TX	K14	-	Keeper
GPIO1_IO02 / USB_OTG2_PWR / TS_YP_YT	TS_YP_YT	Y14	GPIO	Input	GPIO1_IO02	L14	-	Keeper
GPIO1_IO04 / USB_OTG1_PWR / TS_XP_XL	TS_XP_XL	Y15	GPIO	Input	GPIO1_IO04	M16	-	Keeper
BOOT_MODE1	BOOT_MODE1	Y16	GPIO	Input	BOOT_MODE1	U10	-	100 kΩ PD
GPIO1_IO03 / USB_OTG2_OC / TS_XN_XR	TS_XN_XR	Y17	GPIO	Input	GPIO1_IO03	L17	-	Keeper
USB_OTG2_DP	USB_OTG2_DP	Y18	Ana-log	-	USB_OTG2_DP	U13	-	-
USB_OTG1_DN	USB_OTG1_DN	Y19	Ana-log	-	USB_OTG1_DN	T15	-	-

[7] SPI_BOOT_FLASH_EN is used to switch between the onboard SPI flash and external peripherals. For more detailed information about this pin see chapter 7 SPI Flash.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
USB_OTG1_DP	USB_OTG1_DP	Y20	Analog	-	USB_OTG1_DP	U15	-	-
nUSB_OTG1_CHD	USB_OTG1_CHD_B	Y21	GPIO	-	USB_OTG1_CHD_B	U16	-	-
GND	GND	AA1	-	-	-	-	-	-
GND	GND	AA2	-	-	-	-	-	-
NC	Not connected	AA3	-	-	-	-	-	-
NC	Not connected	AA4	-	-	-	-	-	-
NC	Not connected	AA5	-	-	-	-	-	-
NC	Not connected	AA6	-	-	-	-	-	-
SNVS_TAMPER5 / GPIO5_IO5 / ENET1_INT	ENET1_INT	AA7	GPIO	Input	SNVS_TAMPER5	N8	-	Keeper / Not connected[8]
SNVS_TAMPER8 / GPIO5_IO8	GPIO5_IO8	AA8	GPIO	Input	SNVS_TAMPER8	N9	-	Keeper / Not connected[8]
SNVS_TAMPER7 / GPIO5_IO7	GPIO_IO7	AA9	GPIO	Input	SNVS_TAMPER7	N10	-	Keeper / Not connected[8]
UART4_TX / I2C1_SCL	I2C1_SCL	AA10	GPIO	Input	UART4_TX_DATA	G17	3k3 PU to VIO_OUT and connected to PMIC	Keeper
UART3_CTS / CAN1_TX	CAN1_TX	AA11	GPIO	Input	UART3_CTS_B	H15	-	Keeper
UART1_RX	UART1_RX_DATA	AA12	GPIO	Input	UART1_RX_DATA	K16	-	Keeper
UART1_CTS / GPIO1_IO18	GPIO1_IO18	AA13	GPIO	Input	UART1_CTS_B	K15	-	Keeper
GPIO1_IO00 / USB_OTG1_ID / ADC1_IN0	USB_OTG1_ID	AA14	GPIO	Input	PGIO1_IO00	K13	-	Keeper
GPIO1_IO01 / USB_OTG1_OC / TS_YN_YB	TS_YN_YB	AA15	GPIO	Input	GPIO1_IO01	L15	-	Keeper
GPIO1_IO08 / PWM1_OUT / ADC1_IN8	PWM1_OUT	AA16	GPIO	Input	GPIO1_IO08	N17	-	Keeper
GPIO1_IO05 / USDHC1_VSELECT / ADC1_IN5	USB_PWR_EN	AA17	GPIO	Input	GPIO1_IO05	M17	-	Keeper
USB_OTG2_VBUS	USB_OTG2_VBUS	AA18	VBUS Power	-	USB_OTG2_VBUS	U12	-	-
USB_OTG1_VBUS	USB_OTG1_VBUS	AA19	VBUS Power	-	USB_OTG1_VBUS	T12	-	-
CCM_CLK1_N	CCM_CLK1_N	AA20	CCM	-	CCM_CLK1_N	P16	-	-
CCM_CLK1_P	CCM_CLK1_P	AA21	CCM	-	CCM_CLK1_P	P17	-	-

Table 1: Pin assignment

[8] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0]. When the pad is configured as GPIO, the value is keeper out of reset.
SNVS_TAMPER0 to SNVS_TAMPER9 is input unconnected in the following conditions.

- SNVS low power mode when configured as GPIO
- Tamper functions are not used when configured as TAMPER detection pins

It is required to connect external 1M Ohm pull-up or pull-down resistors to the pad to avoid the undesired leakage under two condi-tions above.

3 Power supply and reset

3.1 Power supply

The DHCOR-iMX6UL(L)-01LG has the following power connections:

- VCC_IN_5V = Core module supply voltage input
- VCC_SNVS = Supply for "Secure Non-Volatile Storage" - Voltage output
- VIO_OUT = I/O voltage output
- VCC_CAM = CSI interface supply voltage output
- VCC_SD = SD interface supply voltage output
- VCC_NAND = NAND interface supply voltage output

Notes to VCC_SNVS:

- VCC_SNVS is external needed for booting configuration. Don't use it for other purposes

3.2 Power sequencing

The power output rails start up automatically once VCC_IN_5V is applied to the DHCOR-iMX6UL(L)-01LG. The time until these voltages are available differs between these rails.

- VCC_SNVS = Power on 4 ms after VCC_IN_5V is available
- VIO_OUT = Power on 16 ms after VCC_IN_5V is available
- VCC_CAM = Power on 16 ms after VCC_IN_5V is available
- VCC_SD = Power on 16 ms after VCC_IN_5V is available
- VCC_NAND = Power on 16 ms after VCC_IN_5V is available

4 Reset

The System is put in reset state by holding reset_in signal low.

When the reset_in is asserted, a reset cycle is initiated. The module internal reset and the external reset output POR_B (reset_out) are asserted as long as reset_in is asserted. If the reset input reset_in is deasserted, the POR_B (reset_out) is also deasserted and the module starts booting again.

Notes:

- A 0.1µF capacitor is necessary, even if reset_in is not used on the carrier board. It is also recommended to trigger a reset event (from the carrier board) only via an open-drain circuit. Do not connect reset_in directly to VCC_SNVS.
- A 0.1µF capacitor is necessary, even if POR_B (reset_out) is not used on the carrier board. Do not put any load on the POR_B (reset_out) line.

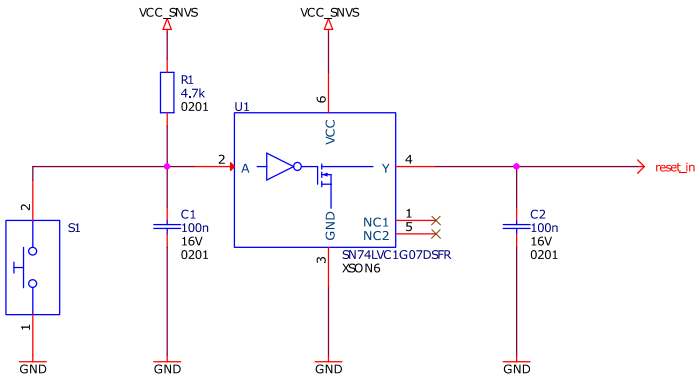

Figure 2: reset_in example

5 Hardware and DDR3 coding

The following pins can be used to read out the current hardware version of the DHCOR-iMX6UL(L)-01LG core module.

CPU ball name	Description	CPU ball number	IO Type
LCD_CLK	Code_HW_0	A8	I
LCD_ENABLE	Code_HW_1	B8	I

Table 2: Hardware coding

DH PCB Numbers	Description	Code_HW_1	Code_HW_0
578-100	HW100 (version 1)	0 (10k PD)	0 (10k PD)
578-200	HW200 (version 2)	0 (10k PD)	1 (10k PU)
578-300	HW300 (version 3)	1 (10k PU)	0 (10k PD)
578-400	HW400 (version 4)	1 (10k PU)	1 (10k PU)

Table 3: Different hardware versions

The following pins can be used to read out the size of the DDR3 memory used on the DHCOR-iMX6UL(L)-01LG core module.

CPU ball name	Description	CPU ball number	IO Type
LCD_HSYNC	Code_RAM_0	D9	I
LCD_VSYNC	Code_RAM_1	C9	I

Table 4: Hardware coding

DDR3 memory size	Code_RAM_1	Code_RAM_0
128 MB	0 (10k PD)	0 (10k PD)
256 MB	0 (10k PD)	1 (10k PU)
512 MB	1 (10k PU)	0 (10k PD)
1 GB	1 (10k PU)	1 (10k PU)

Table 5: Different size of the DDR3 memory

This means the bootloader (U-Boot) scans the states of these pins during start up, starts the correct memory initialization and holds also the information regarding PCB version, to handle PCB differences in the correct way. The coding pins can be used for alternate functions as well, but the customer must remove the pin scanning from bootloader and must ensure to initialize the DDR3 memory with the correct initialization values.

6 JTAG

The standard JTAG and SWD interface is directly available at the following DHCOR pins:

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Pin not used
JTAG_TDO / SAI2_SYNC	JTAG_TDO	K1	SJC	Output	JTAG_TDO	N15	Keeper
JTAG_TRST / SAI2_TXD	JTAG_TRST_B	K2	SJC	Input	JTAG_TRST_B	N14	47 kΩ PU
JTAG_TCK / SAI2_RXD	JTAG_TCK	K3	SJC	Input	JTAG_TCK	M14	47 kΩ PU
JTAG_TDI / SAI2_BCLK	JTAG_TDI	L1	SJC	Input	JTAG_TDI	N16	47 kΩ PU
JTAG_TMS / SAI2_MCLK	JTAG_TMS	L2	SJC	Input	JTAG_TMS	P14	47 kΩ PU
JTAG_MOD	JTAG_MOD	L3	SJC	Input	JTAG_MOD	P15	-

Table 6: JTAG pins

The next figure shows the connection between the DHCOR i.MX6ULL and a standard JTAG connector:

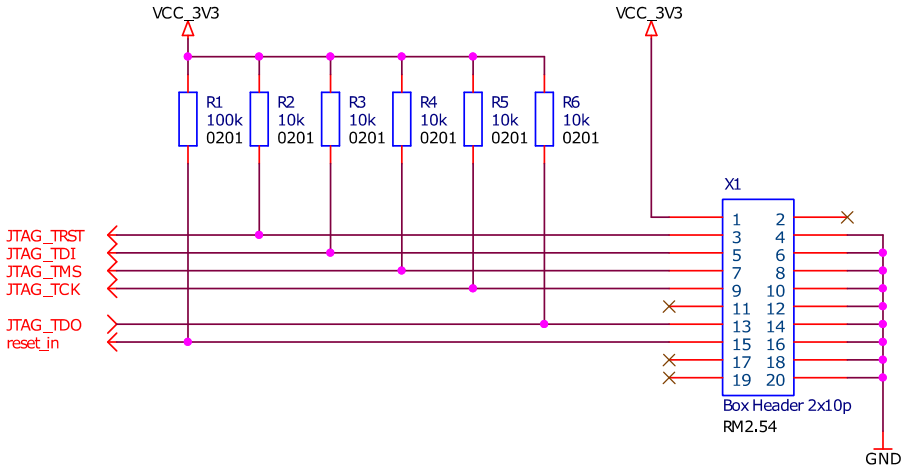

Figure 3: JTAG connection

7 SPI Flash

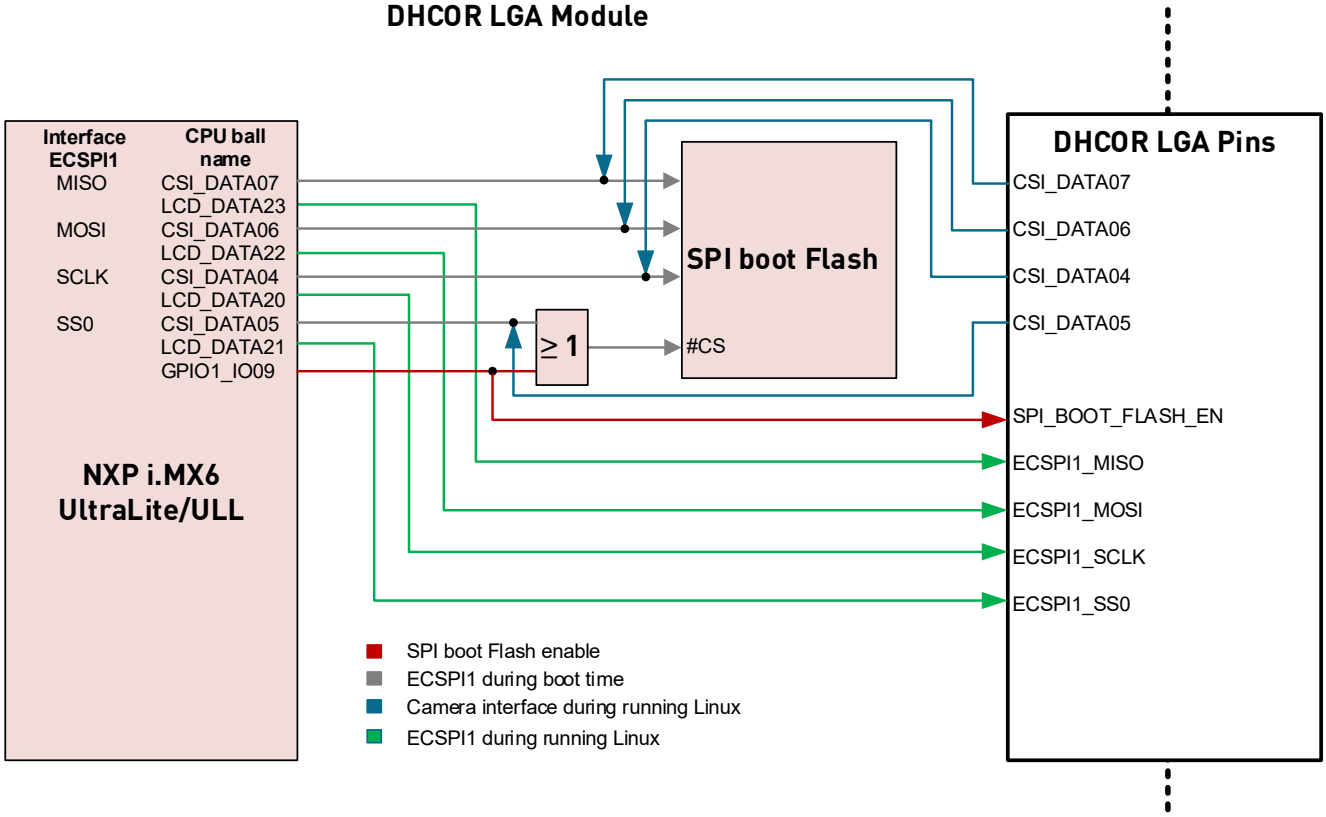

Figure 4: SPI 1 Function Overview

Because of the lack of available pins of the iMX6ULL, the ECSPI1 interface has to be shared with LCD interface and CSI interface. Figure 4 describes how to use these interfaces.

To make sure that the CSI and the external used SPI interfaces ("external" means the SPI port provided at the DHCOR LGA Pins) are disabled during the SPI boot phase it is recommended to use external buffers for the CSI and external SPI interfaces. These buffers could be controlled by the SPI_BOOT_FLASH_EN pin.

This can be archived by using a voltage level translator like shown in Figure 5. Here the TXS0108EPWR (Texas Instruments) is disabled by connecting its OE pin (output enable) to the SPI_BOOT_FLASH_EN pin of the DHCOR-iMX6UL(L)-01LG. During the SPI boot phase SPI_BOOT_FLASH_EN is set to 0 (GND level) which in return sets the outputs of the TXS0108EPWR into a high-impedance state. Therefore, the communication between the CPU and the SPI boot Flash is separated from the CSI interface during the SPI boot phase.

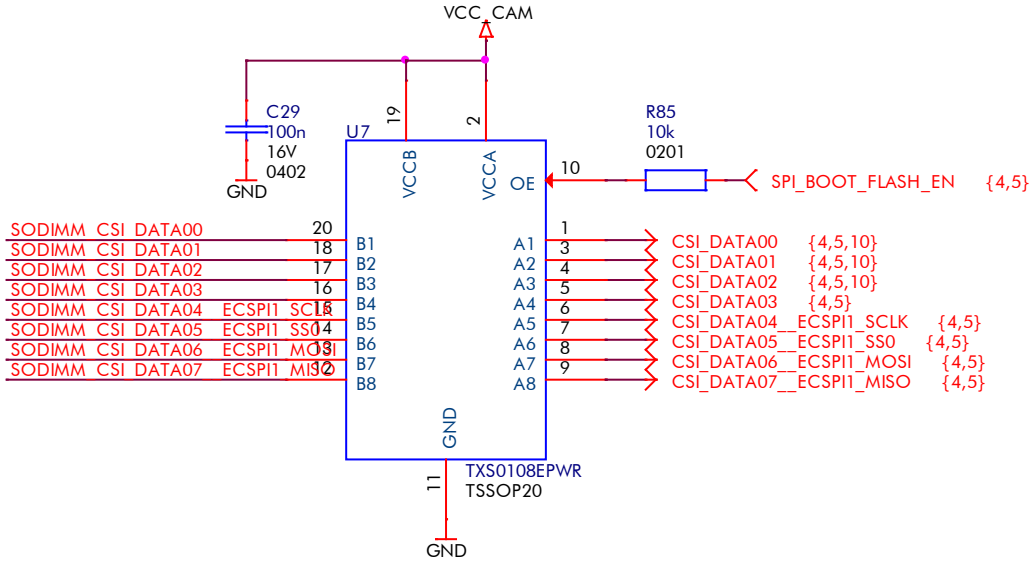

Figure 5: Sample schematic of a buffer for the CSI signals

Summary:

DHCOR without SPI NOR-Flash: In that case the SPI interface, on the CSI_* pins, can be used on the carrier board without any limitations. But it is recommended to use the LCD_* pins for the ECSPI1 interface, because these pins are used from DH electronics reference BSP for this functionality.

DHCOR with SPI NOR-Flash: In case the on module flash is mounted, it is recommended to left the CSI_* pins open at the carrier board design, or to ensure that the CPU has full access to the SPI flash during boot phase (SPI_BOOT_FLASH_EN signal can be used for this). The DHCOR i.MX6UL(L) reference bootloader configures the CSI_* pins for ECSPI1 usage during start up. Before Linux Kernel boot the bootloader set the SPI_BOOT_FLASH_EN pin to 1 and the reference Linux BSP initializes ECSPI1 at the LCD_* pins. This means after Linux boot, there is no access to the SPI boot NOR-Flash anymore and ECSPI1 is available at the LCD_* pins without any limitations.

8 I²C™

Only I2C1 is fixed to the I2C functionality, because the PMIC DA-9061 is connected to this interface. It can be accessed via the addresses 0x58 and 0x59.

Therefore, also the pull-up resistors to VIO_OUT are located at the DHCOR module. For all other I2C interfaces no pull-up resistors are added to the signals on the DHCOR module. This means, the signals can be used for alternate functions as well.

LGA pin name	Description	LGA pin number	IO Type	CPU ball number	CPU ball name	CPU mux func. name	Not used
UART4_TX / I2C1_SCL	I²C clock line (CLK)	AA10	IO	G17	UART4_TX_DATA	I2C1_SCL	-
UART4_RX / I2C1_SDA	I²C data line (CLK)	W11	IO	G16	UART4_RX_DATA	I2C1_SDA	-

Table 7: I2C1 interface

9 Boot Mode

The DHCOR-iMX6UL(L)-01LG module provides three different modes to boot. To select a specific one, the pins BOOT_MODE0 and BOOT_MODE1 needs to be connect to either GND for a logic 0 or to VCC_SNVS for a logic 1. When connecting the pins to VCC_SNVS use a 10k Ohm pull-up resistor.

It is important to use VCC_SNVS, because this is the first voltage to be generated by the DHCOR-iMX6UL(L)-01LG module and therefore this assures that the CPU is able to sample the boot configuration at its power up.

BOOT_MODE1	BOOT_MODE0	Description
0	0	Boot from Fuses.
0	1	Serial Downloader
1	0	Internal Boot

Table 8: Selection of different Boot Modes

The DH default configuration for the boot mode is "Internal Boot" which uses the on board SPI flash. But this configuration is NOT set with pull-up and pull-down resistors at the DHCOR module. This MUST be done on the carrier board. So please ensure, that the pins are connected at your design.

Beside this BOOT_MODE pins there are different BT_CFG pins available. With these pins it is possible to select the desired boot source. The DH standard boot source is serial NOR-Flash boot from the DHCOR SPI Flash.

Also, here the default configuration is NOT set with pull-up and pull-down resistors at the DHCOR module. This MUST be done on the carrier board. So please ensure, that the pins are connected at your design.

The LCD_* pins are shared with the BT_CFG functionality:

LGA pad name	LGA pad number	Ball Type	Input/ Output	CPU ball name	BT_CFG pin	DHCOR SPI boot mode
LCD_DATA07	M20	GPIO	Input	LCD_DATA07	BT_CFG1[7]	PD 10 kΩ
LCD_DATA06	E21	GPIO	Input	LCD_DATA06	BT_CFG1[6]	PD 10 kΩ
LCD_DATA05	H19	GPIO	Input	LCD_DATA05	BT_CFG1[5]	**PU 10 kΩ**
LCD_DATA04	K20	GPIO	Input	LCD_DATA04	BT_CFG1[4]	**PU 10 kΩ**
LCD_DATA03	M19	GPIO	Input	LCD_DATA03	BT_CFG1[3]	PD 10 kΩ
LCD_DATA02	P19	GPIO	Input	LCD_DATA02	BT_CFG1[2]	PD 10 kΩ
LCD_DATA01	E20	GPIO	Input	LCD_DATA01	BT_CFG1[1]	PD 10 kΩ

LGA pad name	LGA pad number	Ball Type	Input/ Output	CPU ball name	BT_CFG pin	DHCOR SPI boot mode
LCD_DATA00	G21	GPIO	Input	LCD_DATA00	BT_CFG1[0]	PD 10 kΩ
LCD_DATA15	N19	GPIO	Input	LCD_DATA15	BT_CFG2[7]	PD 10 kΩ
LCD_DATA14	F20	GPIO	Input	LCD_DATA14	BT_CFG2[6]	PD 10 kΩ
LCD_DATA13	H21	GPIO	Input	LCD_DATA13	BT_CFG2[5]	PD 10 kΩ
LCD_DATA12	K21	GPIO	Input	LCD_DATA12	BT_CFG2[4]	PD 10 kΩ
LCD_DATA11	M21	GPIO	Input	LCD_DATA11	BT_CFG2[3]	PD 10 kΩ
LCD_DATA10	P20	GPIO	Input	LCD_DATA10	BT_CFG2[2]	PD 10 kΩ
LCD_DATA09	F19	GPIO	Input	LCD_DATA09	BT_CFG2[1]	PD 10 kΩ
LCD_DATA08	H20	GPIO	Input	LCD_DATA08	BT_CFG2[0]	PD 10 kΩ
LCD_DATA23 / ECSPI1_MISO	J20	GPIO	Input	LCD_DATA23	BT_CFG4[7]	PD 10 kΩ
LCD_DATA22 / ECSPI1_MOSI	G19	GPIO	Input	LCD_DATA22	BT_CFG4[6]	PD 10 kΩ
LCD_DATA21 / ECSPI1_SS0	J21	GPIO	Input	LCD_DATA21	BT_CFG4[5]	PD 10 kΩ
LCD_DATA20 / ECSPI1_SCLK	L20	GPIO	Input	LCD_DATA20	BT_CFG4[4]	PD 10 kΩ
LCD_DATA19	N20	GPIO	Input	LCD_DATA19	BT_CFG4[3]	**PU 10 kΩ**
LCD_DATA18	F21	GPIO	Input	LCD_DATA18	BT_CFG4[2]	PD 10 kΩ
LCD_DATA17	J19	GPIO	Input	LCD_DATA17	BT_CFG4[1]	PD 10 kΩ
LCD_DATA16	L19	GPIO	Input	LCD_DATA16	BT_CFG4[0]	PD 10 kΩ

Table 9: BT_CFG pins

For more information regarding BT_CGF pins, we refer you to the website of NXP https://www.nxp.com/

Notes:

- How to set default boot mode (SPI boot) on your carrier board design:

  BOOT_MODE1 (DHCOR Pin Y16) = 10k pull-up to VCC_SNVS

  BOOT_MODE0 (DHCOR Pin W16) = 10k pull-down to GND

  SPI boot (DH default for DHCOR SPI boot):

  LCD_DATA04 / BT_CFG1[4] = 10k pull-up to VCC_SNVS (DHCOR Pin K20)

  LCD_DATA05 / BT_CFG1[5] = 10k pull-up to VCC_SNVS (DHCOR Pin H19)

  LCD_DATA19 / BT_CFG4[3] = 10k pull-up to VCC_SNVS (DHCOR Pin N20)

  For all other boot modes, please have a look at NXP documentation.

  Note: VCC_SNVS = DHCOR Pin A15
- With a specific bootloader command the configuration can be programmed to the eFuses (see NXP reference manual for further information's). In all further boot processes the eFuses are read at power up instead of the Boot config pins.

10 UART for bootloader and Linux console

It is strongly recommended to use one UART interface to enable access to the bootloader and linux console on the carrier board. The port can be deactivated during production to avoid illegal access to the series device, but for development and prototyping this port should be accessible.

DH electronics recommends to use the following pins for bootloader and linux console, because these pins are used from DH electronics reference BSP for this functionality:

- Y13: UART1_TX
- AA12: UART1_RX

11 WiFi / Bluetooth

The DHCOR-iMX6UL(L)-01LG system-on-module provides a 2.4GHz wireless local area network (WLAN) and Bluetooth (BT) solution via the Murata 1DX module as an option. Based on Cypress CYW4343W, the module provide high-efficiency RF front end circuits. The module is designed to fit into small spaces.

- **WiFi:** IEEE802.11b/g/n W-LAN
- **Bluetooth:** Bluetooth® v4.1 (BR/EDR/BLE)

The module has one antenna port, via a dedicated U.FL connector.

LGA pin name	Description	LGA pin number	IO Type	1DX pin number	1DX pin name	Not used
BT_DEV_WAKE	Device wake up signal	D2	IO	39	BT_DEV_WAKE	
BT_HOST_WAKE	Host wake up signal	D3	IO	38	BT_HOST_WAKE	
BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	E1	I	14	BT_REG_ON	
WL_HOST_WAKE	-	E2	-	27	WL_GPIO_0_ HOST_WAKE	
WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	E3	I	28	WL_REG_ON	
UART2_TX	UART serial input. Serial data input for the HCI UART interface.	F1	I	2	BT_UART_RXD	
UART2_RX	UART serial output. Serial data output for the HCI UART interface.	F2	O	3	BT_UART_TXD	
LPO_IN_32kHz	External sleep clock input (32.768kHz).	F3	I	37	LPO_IN (32kHz)	
UART3_TX / UART2_CTS	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	G1	I	4	BT_UART_CTS_N	

LGA pin name	Description	LGA pin number	IO Type	1DX pin number	1DX pin name	Not used
UART3_RX / UART2_RTS	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.	G2	O	5	BT_UART_RTS_N	
BT_GPIO_4		M1	-	7	BT_GPIO_4	
BT_GPIO_3		M2	-	6	BT_GPIO_3	
WL_GPIO_4		M3	-	15	WL_GPIO_4	
WL_GPIO_1		N1	-	18	WL_GPIO_1	
WL_GPIO_2		N2	-	17	WL_GPIO_2	
BT_I2S_DO		N3	-	16	BT_I2S_dO	
BT_GPIO_5		P1	-	13	BT_GPIO_5	

Table 10: WiFi/BT signals

Notes:

- As a request the WiFi / Bluetooth module can be connected to the audio interface.
- At the carrier board design, it is necessary to source the LPO_IN_32kHz pin from an external oscillator. Furthermore, it is mandatory to connect the WL_REG_ON and BT_REG_ON pins to i.MX6ULL GPIO's, because these pins must be activated during power up.

  It is recommended to use UART1_CTS / GPIO1_IO18 and SNVS_TAMPER9 / GPIO5_IO9, because these pins are used from DH electronics reference BSP for the REG_ON functionality.

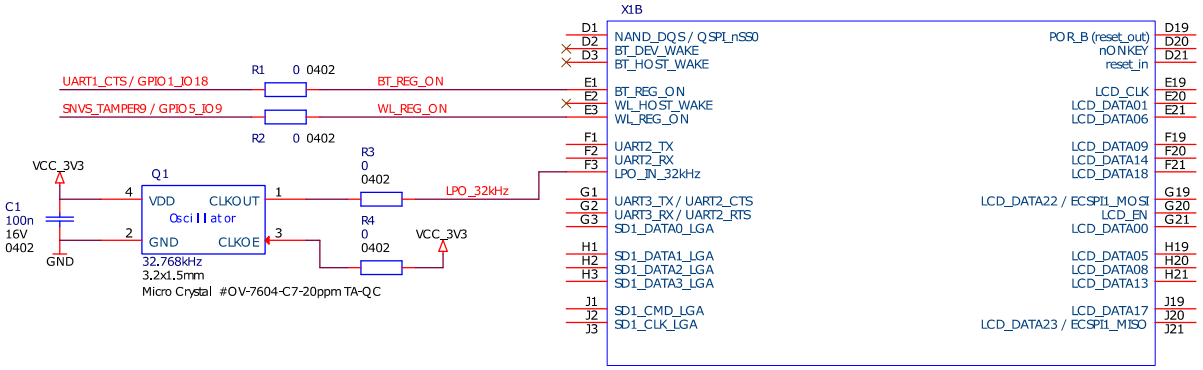

Figure 6: Carrier board connections for WiFi/BT functionality

12 eMMC connection

The external eMMC connection is a little bit tricky, because of the small eMMC housing pitch of 0.5 mm. But with the following instruction's it is possible to connect an eMMC with a standard 4-layer PCB with through hole vias and line width and spacing parameters of 0.120 mm. The main idea is to use unconnected pins for routing.

Note the following example is based on eMMC5.1 JEDEC standard. Fortunately, the newer eMMC devices are backward compatible with the older eMMC specifications. The standard contains VSF, NC and RFU pins. The NC pins can be routed through while the RFU pins should be avoided during routing.

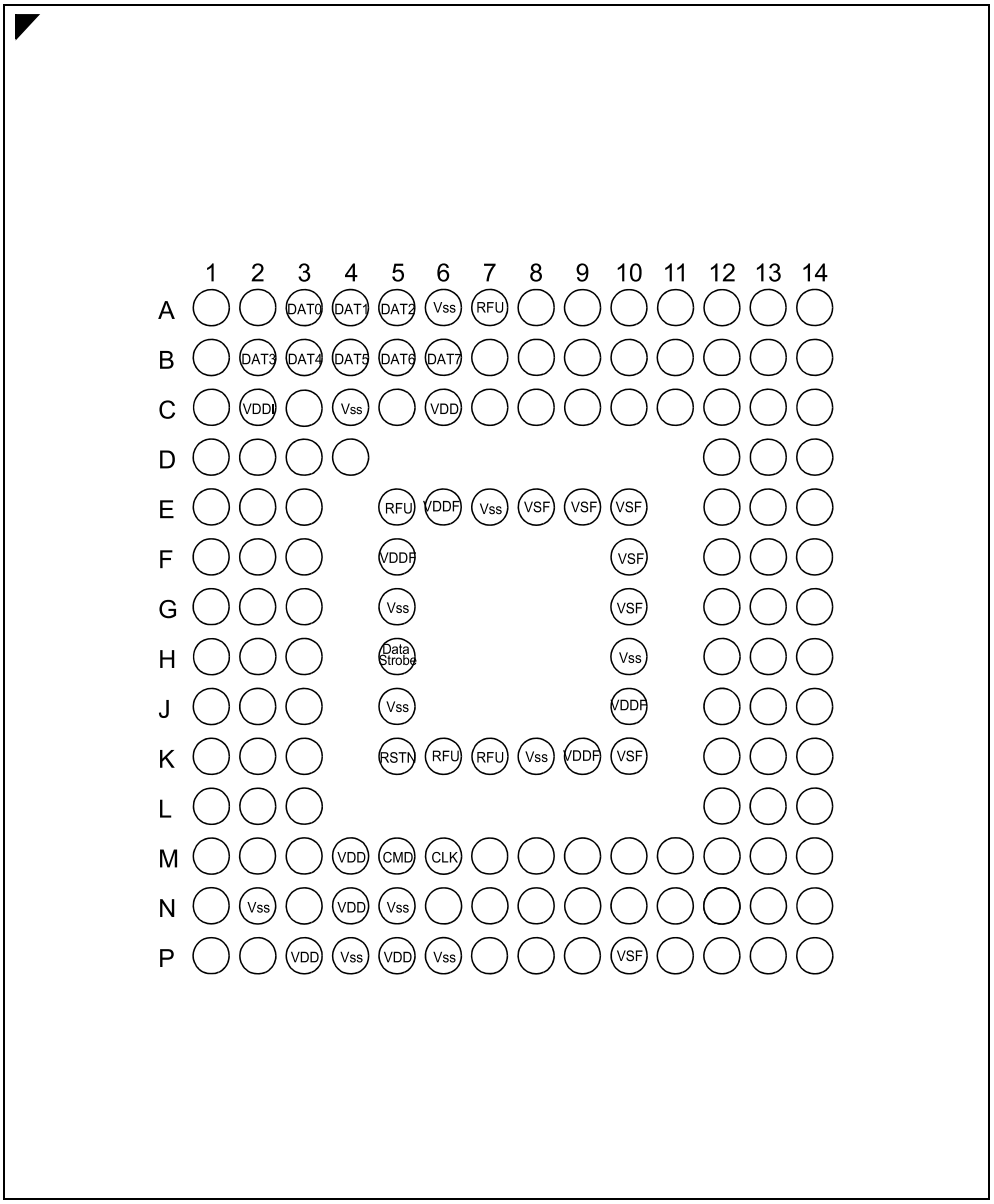

Figure 7: eMMC pinout (153 nall BGA), based on eMMC5.1 JEDEC standard

Pin number	Name	Description
A3	DAT0	Bidirectional data channel DAT0
A4	DAT1	Bidirectional data channel DAT1
A5	DAT2	Bidirectional data channel DAT2
B2	DAT3	Bidirectional data channel DAT3
B3	DAT4	Bidirectional data channel DAT4
B4	DAT5	Bidirectional data channel DAT5
B5	DAT6	Bidirectional data channel DAT6
B6	DAT7	Bidirectional data channel DAT7
K5	RSTN	H/W reset signal pin
C6, M4, N4, P3, P5	VDD	Supply voltage for memory controller

Pin number	Name	Description
E6, F5, J10, K9	VDDF	Supply voltage for flash memory
C2	VDDI	Internal power node to stabilize regulator output to controller core logics
M5	CMD	A bidirectional signal used for device initialization and command transfers.
H5	Data Strobe	Newly assigned pin for HS400 mode. Data Strobe is generated from e.MMC to host.
M6	CLK	Clock input
J5, A6, C4, E7, G5, H10, K8, N2, N5, P4, P6	VSS	Ground connections

Table 11: eMMC pin description

Figure 8 below shows the eMMC schematic example of DHCOR-iMX6UL(L)-01LG connected to an eMMC v5.1 device. All of the reserved and additional pins are designated on the schematic symbol, only the not connected pins are left away, so it is easier to understand and avoid those pins in layout.

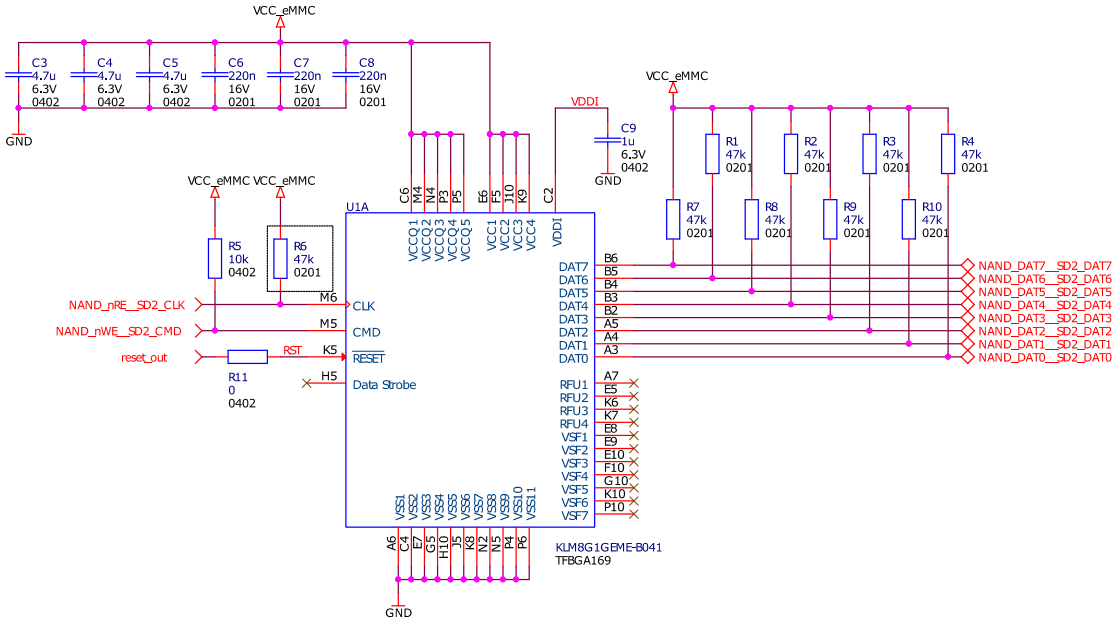

Figure 8: eMMC schematic example

Figure 9 shows an example routing of a v5.1 eMMC device using 0.12 mm trace / 0.12 mm space routing and 0.3 mm drill / 0.65 via pad.

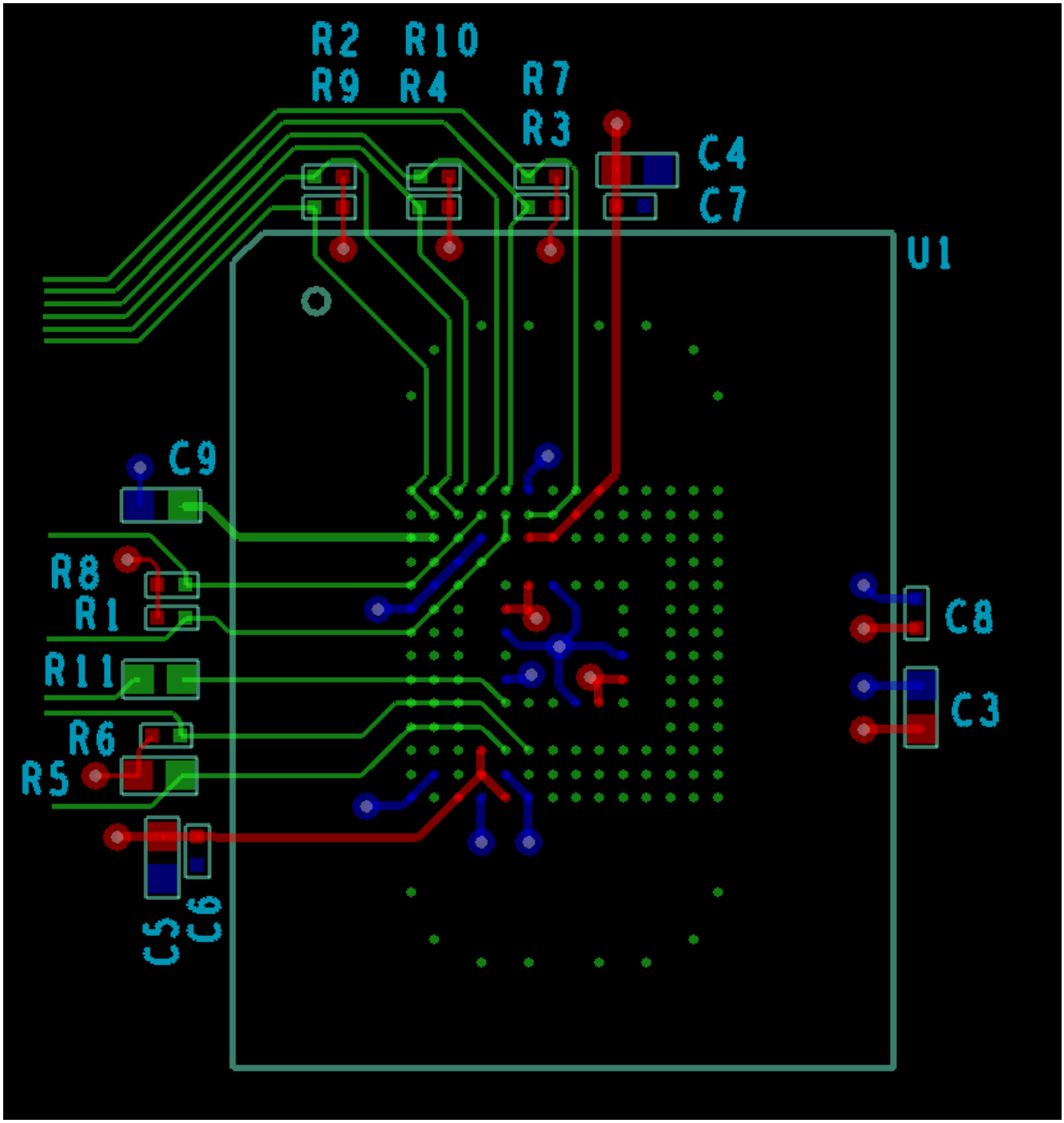

Figure 9: eMMC routing example

Note: The eMMC lines (CMD, CLK and DAT*) should be routed with matched trace lengths.

13 Technical specifications

13.1 Operating conditions – Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit
VCC_IN_5V	Power supply voltage INPUT	4.2	5.0	5.5	V
VCC_IN_5V$_{ripple}$	VCC ripple peak-to-peak	-	30	60	mV
VCC_CAM	Camera voltage OUTPUT	-	3.3	-	V
I$_{VCC_CAM}$	VCC_CAM current	-	-	100	mA
VCC_SD	SD voltage OUTPUT	-	3.3	-	V
I$_{VCC_SD}$	VCC_SD current	-	-	250	mA
VCC_NAND	NAND voltage OUTPUT	-	3.3	-	V
I$_{VCC_NAND}$	VCC_NAND current	-	-	250	mA
VIO_OUT	I/O voltage OUTPUT	-	3.3	-	V
I$_{VIO_OUT}$	VIO_OUT current	-	-	600	mA
VCC_SNVS	VCC_SNVS is external needed for booting configuration. Don't use it for other purposes	-	3.3	-	V
I$_{VCC_SNVS}$	VCC_SNVS current	-	-	100	mA
P$_{Operating}$ (Power)	Core module power consumption	-	0,6[9]	1,5[9] 3,0[9] (with WiFi)	W W
VIH_3V3	Digital input high voltage	2.0	3.3	-	V
VIL_3V3	Digital input low voltage	-	0	0.8	V

Table 12: DC operating conditions

13.2 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
reset_in	System Reset input assertion time (active low)	10			ms
POR_B (reset_out)	System Reset output assertion time (active low)	10			ms

Table 13: Reset Timings

13.3 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C
T_AMB	Operating temperature range **with Murata 1DX (WiFi/BT)**	-30		70	°C

Table 14: Temperature range

Figure 10 shows the temperature conditions on the DHCOR iMX6ULL module with 900MHz under full load and with WiFi communication.

Test conditions:

- Iperf WiFi test (DHCOR i.MX6ULL WiFi module 1DX → Fritzbox with iperf server): `iperf -c 192.168.188.1 -p 4711 -t 100000`

[9] Only DHCOR module, without any output power on VIO_OUT, ...

Iperf Result: 24.7 Mbit/s

- CPU stress test: `stress-ng --cpu 1 &`
- VIO_OUT: External load with 600mA at 3V3 is connected.

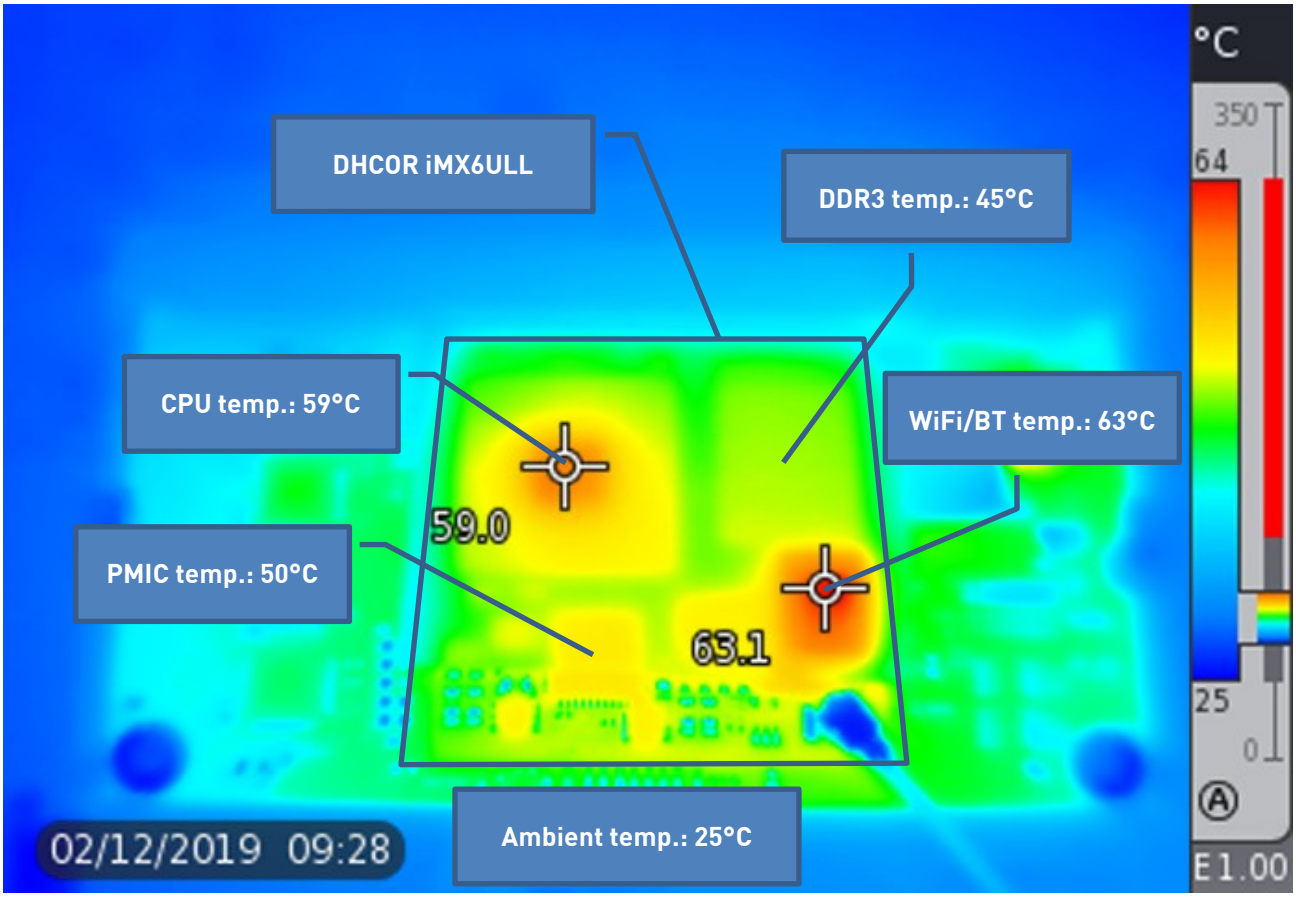

Figure 10: Temperature example (i.MX6ULL at 900MHz with WiFi communication) at full load

14 Mechanical specifications

14.1 Dimensions

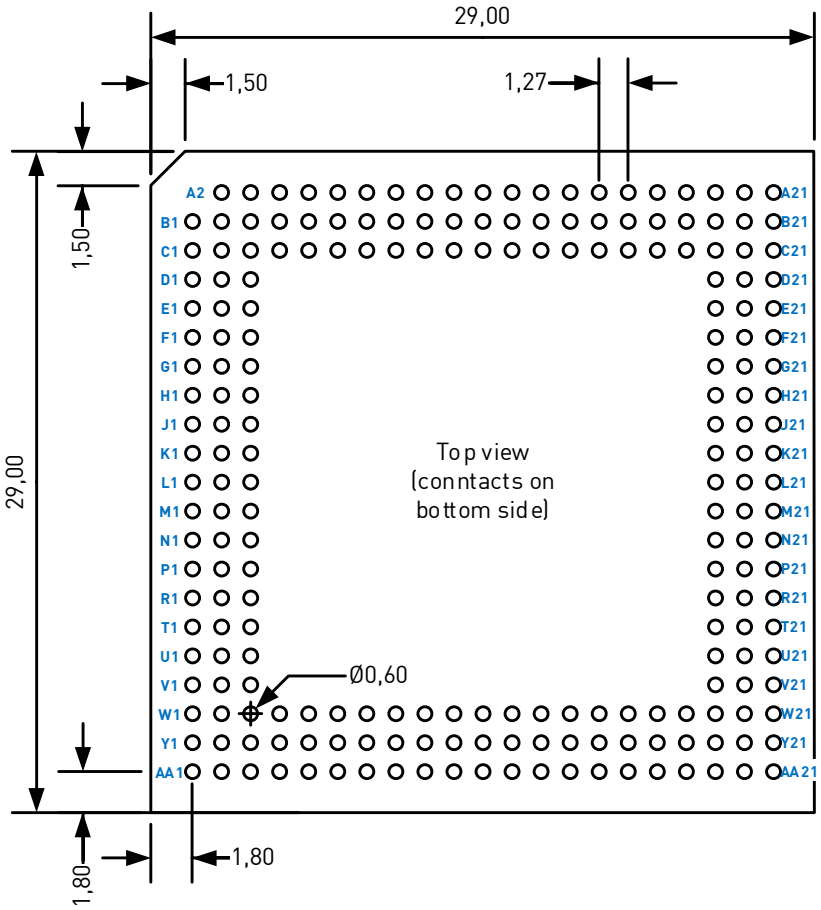

Figure 11: Dimensions of the module

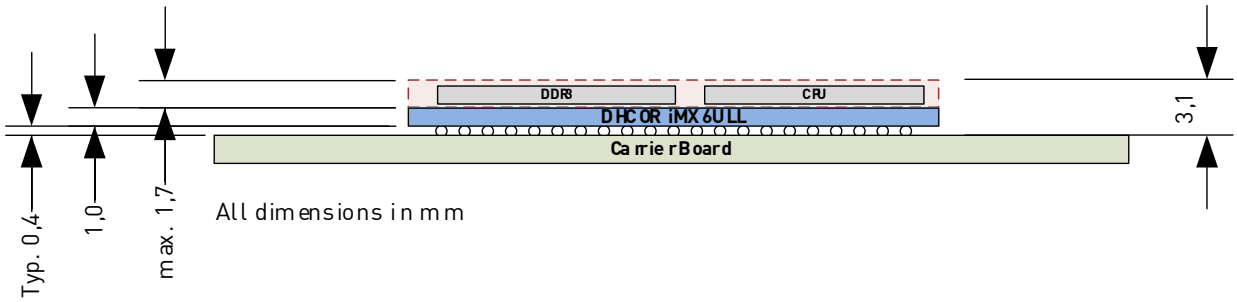

Figure 12: DHCOR height

15 Assembly instructions

DHCOR-iMX6UL(L)-01LG has been designed for SMT mounting of the module on the carrier board. The DHCOR uses LGA contact pads on the bottom side for the connection to the carrier board. During the production process of the module solder paste is applied to the LGA pads. Therefore, the DHCOR is nearly similar to a BGA. The solder paste on the pads improves the contact quality between module and carrier board, compared with a standard LGA part (without solder paste on the module pads).

15.1 Moisture sensitivity and shelf life

- Calculated shelf life in tape and real packaging: 12 months at < 40 °C and < 90 % relative humidity (RH).
- The DHCOR-iMX6UL(L)-01LG is applicable to MSL3 (based on IPC/JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at < 30 °C and < 60 % RH and the product shall be used within 168 hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 $^{+5}/_{-0}$ °C, 24 hours, 1 time
- The products shall be baked on a heat-resistant tray since the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

15.2 Coplanarity

Coplanarity of the carrier board: < 0.1 mm

15.3 Solder pastes

Solder paste parameters:

- Any lead-free (Pb-free) SAC solder pastes can be used.

Solder paste print parameters:

- Stencil thickness: > 0.1 mm (recommended 0.15 mm)
- Stencil pad diameter: Suggestion 0.55 mm (0.6 mm pad size)

15.4 Reflow Process

Use reflow profiles per IPC/JEDEC J-STD-020D.

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_L)	 150 °C 200 °C 60-120 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60-150 °C
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6°C/second max.
Time 25 °C to peak temperature	8 minutes max.

Table 15: Reflow profil per IPC/JEDEC J-STD-020E

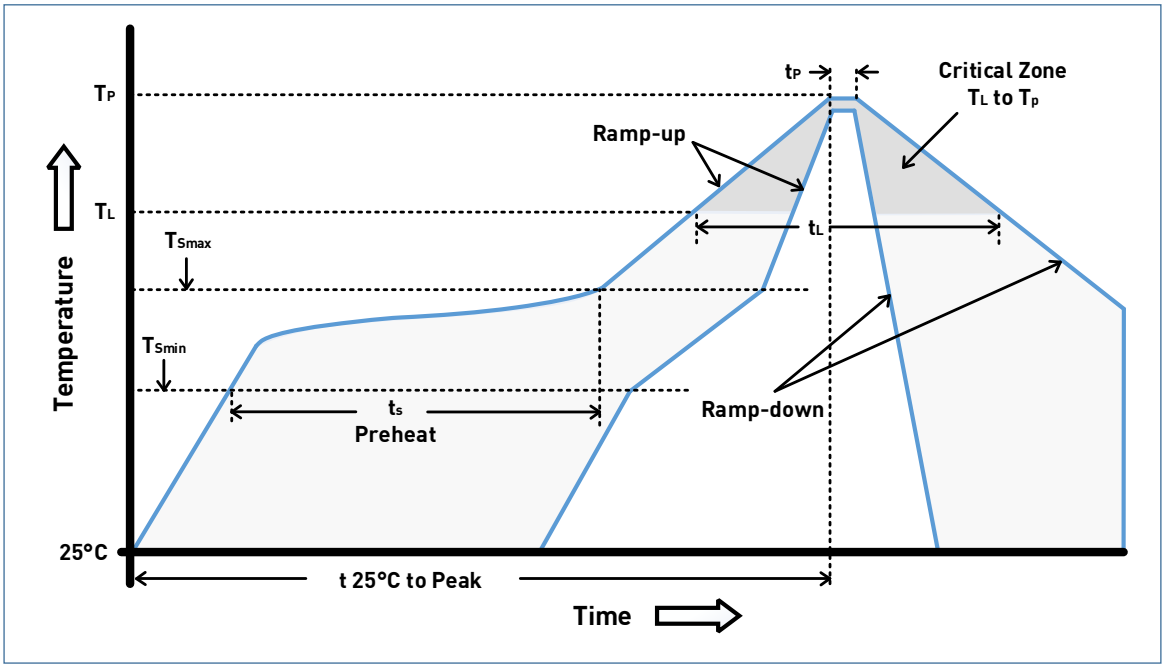

Figure 13: Reflow Classification Profile

The manufacturing of the DHCOR-iMX6UL(L)-01LG requires two reflow cycles. Two reflow cycles are remaining for mounting the module on the carrier board. It is strongly recommended to solder the DHCOR-iMX6UL(L)-01LG module during the last reflow cycle of the carrier board manufacturing process.

16 Tape and reel packaging

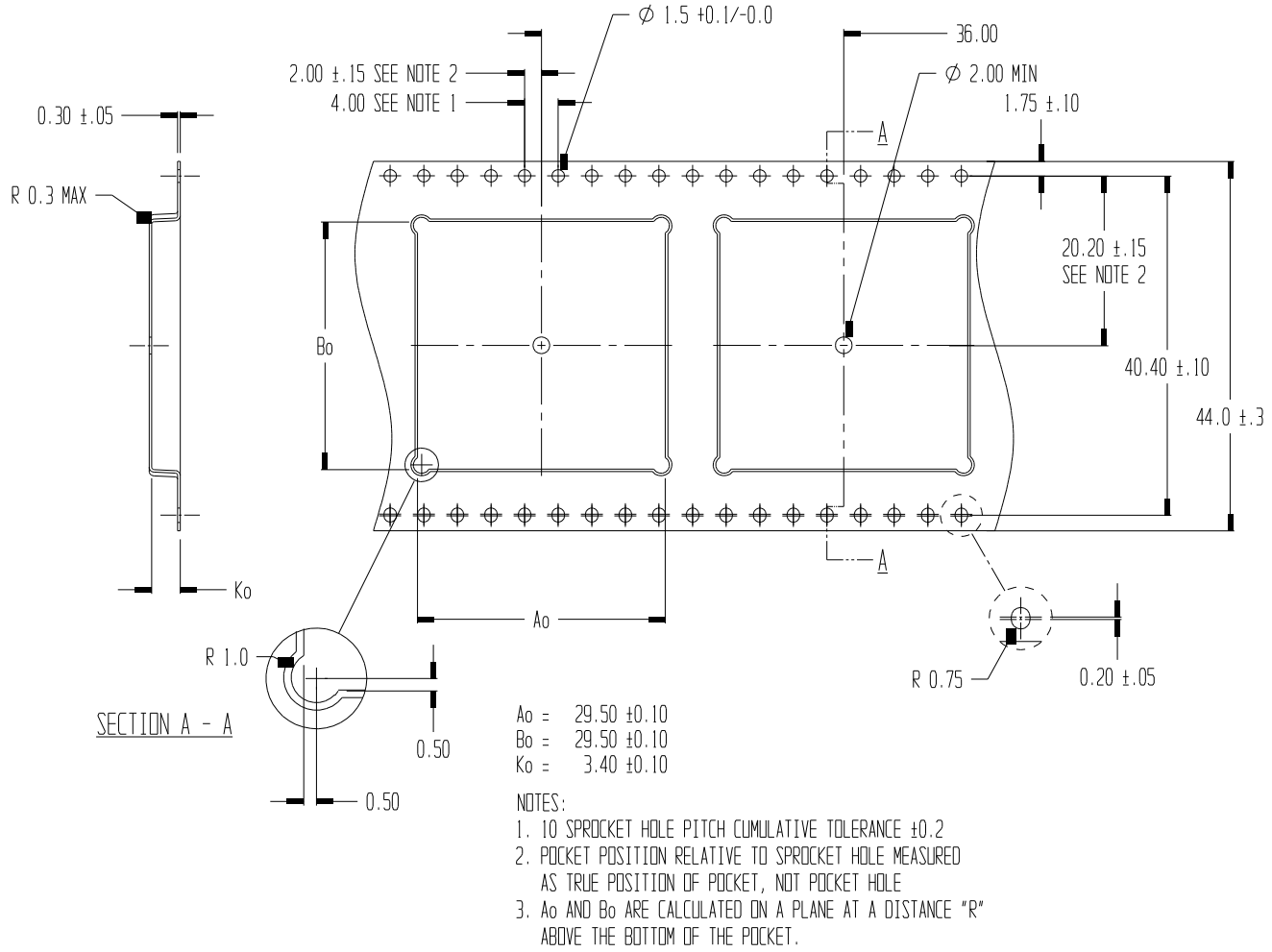

Figure 14: Tape and reel packaging

17 Hardware design checklist

Table 16 is a checklist for all the important design guidelines. Please read each checklist entry carefully to ensure that your carrier board design meets these guidelines.

Number	Checklist / Design notes
1	It is recommended to reuse the DH electronics default pin functionality as far as possible in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can be taken from the reference BSP, without any Device Tree porting efforts. Please have a look at "DH electronics default function" at chapter 2.2 Pin assignment

Number	Checklist / Design notes
2	Make sure the boot mode pins are connected properly at the carrier board design. Please have a look at chapter 9 Boot Mode
3	Does the carrier board design provide any connection to the JTAG pins (e.g. mounting option, only for development)? Please have a look at chapter 6 JTAG
4	If a DHCOR variant with WiFi/BT is used, it is mandatory to connect LPO_IN_32kHz, WL_REG_ON and BT_REG_ON pins on the carrier board design in the correct way. Please have a look at chapter 11 WiFi / Bluetooth
5	Does the carrier board design provide any serial connection to bootloader and Linux console? Please have a look at chapter 10 UART for bootloader and Linux console
6	Ensure correct reset_in and POR_B (reset_out) connection. Please have a look at chapter 4 Reset
7	Ensure, that the CPU has full access to the SPI NOR-Flash during start up, if you are using a DHCOR variant with mounted SPI boot flash. Please have a look at chapter 7 SPI Flash
8	Some LCD_* pins are used from the reference BSP to recognize the DHCOR hardware version and the memory size. These pins can be used for LCD_* functionality, but it is not recommended to add any pull-up or pull-down resistors to the carrier board design. If these pins will be used for other functionality on the carrier board, the customer must adjust the hardware and DDR3 size detection in the reference bootloader. Please have a look at chapter 5 Hardware and DDR3 coding

Table 16 Hardware design checklist

18 RoHS conformance

This device has been manufactured RoHS II-compliant.