



DHCOM I.MX6UL(L)

User Manual

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THE ART OF INNOVATION

Changes

| Version | Date | Changes | Name |
|----------------|-------------|----------------------------------|-------------|
| R01 | 2018-04-10 | First version | KH |
| R01 | 2018-04-23 | Reviewed and released | AG |
| R02 | 2020-03-31 | Changed Bluetooth Version to 5.1 | MAD |

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Abbreviations

- AIN = Analog input
- AINOUT = Analog input/output
- I = Input
- IO = Input/output
- MBC = Must be connected
- O = Output
- PD = Pull-Down
- PU = Pull-Up
- PWR_I = Power input
- PWR_O = Power output
- TBD = To be defined

1 Introduction

1.1 Hardware

The DHCM-iMX6UL(L)-01D2 module is a computer module in the SODIMM-200 form factor on the basis of a Cortex-A7 processor from NXP. The CPU is clocked up to 900 MHz and is equipped with up to 1 GByte DDR3-Memory and 16 GByte eMMC flash. Numerous interfaces are also available for communicating with the outside world, which are required in embedded systems.

The pin assignment of the SODIMM 200 socket is subject to the DHCOM standard, so that a replacement or an upgrade to other DHCOM modules is very easily possible.

1.2 Software

At present, the DHCM-iMX6UL(L)-01D2 module is available with the Embedded Linux operating system.

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.

1.3 Main characteristics

- Cortex-A7 NXP i.MX6UL(L) up to 900 MHz
- Absolute power efficient and cost optimized application processor
- Crypto Engine, Secure Boot
- 128 - 1024 MByte NAND flash memory (8 bit bus width) or 4 - 16 GByte eMMC flash
- 2 MByte SPI boot flash
- 128 - 1024 MByte DDR3 memory
- On-board microSD card socket¹
- MMC 4.5 / SD 3.0 / SDIO Port (1-/2-/4-bit)
- LC display controller, 18 bit colors, max. 1366x768 pixels
- CSI parallel camera interface, 8 bit / pixel data format
- On-board touch controller for 4-wire resistive touch screens
- Ethernet controller 10/100 Mbit, IEEE1588 conform
- Ethernet controller 10/100 Mbit, IEEE1588 conform²

¹ DHCOM MMC/SD is only available if microSD socket and Wifi is not mounted. Also on module microSD socket is only available if Wifi is not mounted.

² Second Ethernet controller is only available if SPI2 is not used.

- USB 2.0 OTG high-speed
- USB 2.0 host high speed
- UART 1, Rx / Tx, up to 5.0 Mbit/s
- UART 2, Rx / Tx / Rts / Cts, up to 5.0 Mbit/s
- CAN 1, V2.0B, 1 Mbit/s
- CAN 2, V2.0B, 1 Mbit/s
- SPI 1, max. 52 Mbps
- SPI 2, max. 52 Mbps³
- I2C™ 1, max. 400 kbit
- I2C™ 2, max. 400 kbit
- I²S Audio interface⁴
- Real-time clock RTC
- 2x 10 bit ADC with 3.3V reference voltage
- 2x 256 byte EEPROM with integrated MAC address
- PWM 1x 16 bit
- 9 GPIOs
- JTAG debug connection via FFC plug connector
- Industrial temperature range (-40°C to +85°C)
- SODIMM-200 socket with DHCOM pin assignment

1.4 CPU differences

For more information and differences between i.MX6ULL and i.MX6UltraLite processor, we refer you to the website of NXP <https://www.nxp.com/>

1.5 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

1.5.1 NXP i.MX6ULL processor

Data sheets and technical documents can be found at <https://www.nxp.com/>

1.5.2 Microchip ethernet PHY LAN8710Ai

Data sheets and technical documents can be found at <https://www.microchip.com/>

³ SPI 2 is only available if ethernet 2 is not mounted

⁴ I2S lines are shared with JTAG

1.5.3 Micro Crystal real-time clock RV-8803-C7

Data sheets and technical documents can be found at <http://www.microcrystal.com/>

1.5.4 Analog Digital Converter

Data sheets and technical documents can be found at <http://www.ti.com/>

1.5.5 PMIC

Data sheets and technical documents can be found at <https://www.dialog-semiconductor.com/>

1.5.6 WiFi/BT

Data sheets and technical documents can be found at <https://wireless.murata.com>

2 Hardware overview

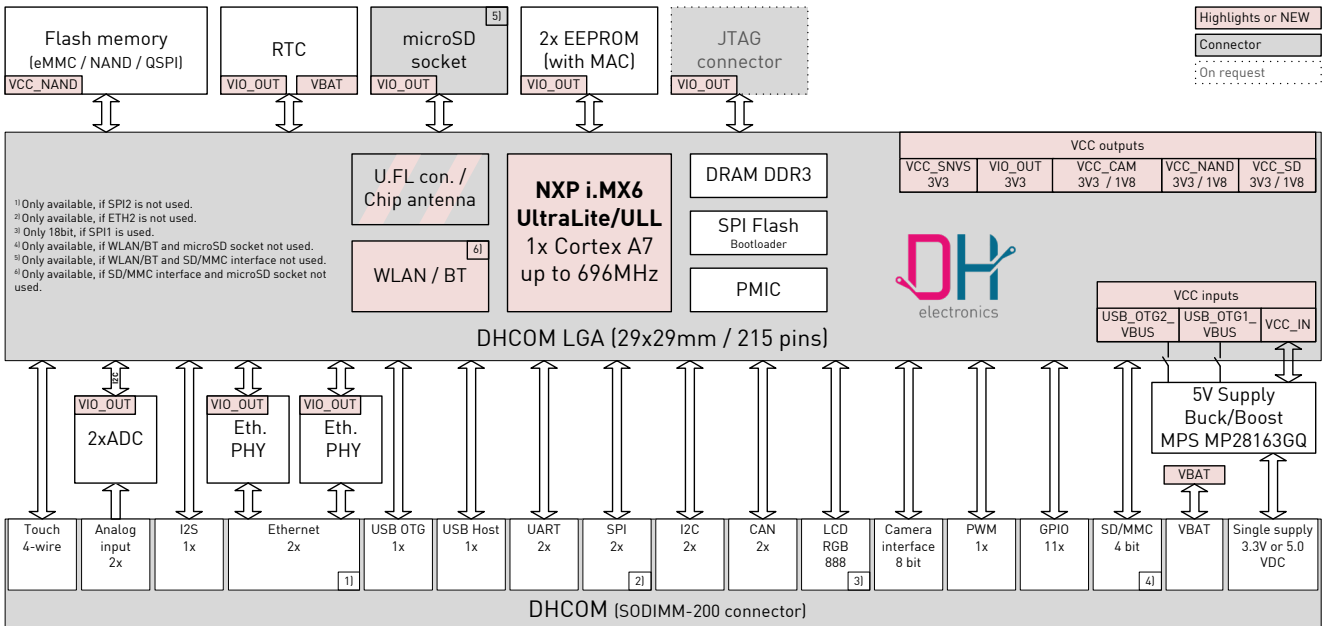


Figure 1: DHCM-iMX6UL(L)-01D2 block diagram

3 Signal description

The following subsections describe the signals at the SODIMM-200 socket.

Notes:

- For all specified pull-up and pull-down resistors, a value of 10k is recommended.
- “Not used” specification describes, what needs to be done with unconnected pins.

DHCOM hardware compatibility:

The DHCOM specification specifies function groups in order to ensure compatibility between various DHCOM modules. Each function group has its own voltage level output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters on the customer specific main board provide compatibility between various DHCOM modules. Naturally, these level shifters can also be removed from the customer design. In this case, the customer will lose compatibility to the DHCOM standard.

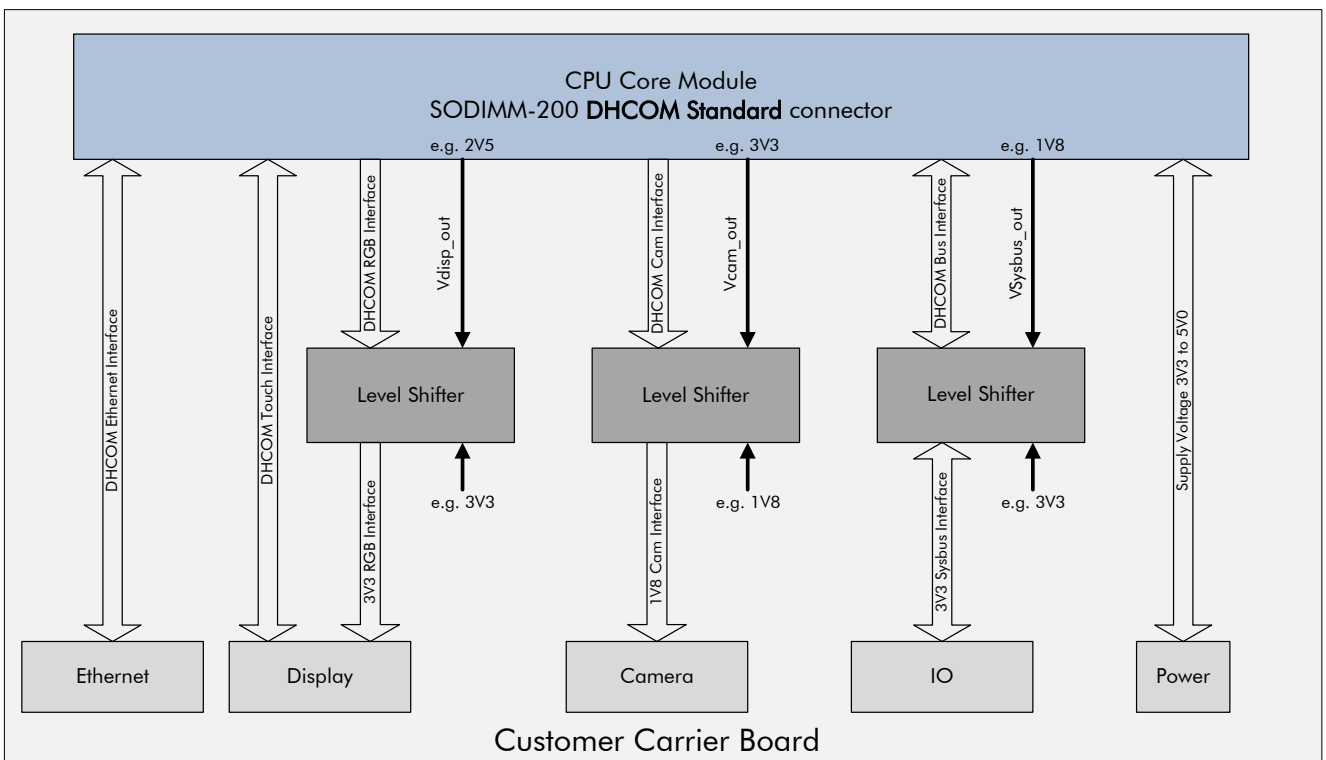


Figure 2: DHCOM functions groups concept

Important:

With the level shifter concept it is possible to support all core modules which are developed from DH electronics in the future. If you only like to use the current DHCOM modules (DHCOM i.MX25, AM35x, i.MX6 and AM335x) you only need to use level shifters in special cases, if you have a look at the following table:

| Voltage | i.MX25 | i.MX6UL(L) | AM35x | AM335x | i.MX6 | SD600E |
|-------------------|-------------|-------------|-------------|-------------|-------------|-------------|
| VCC (Vin) | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V |
| Vbat | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V |
| Vsysbus | 1.8V | - (3.3V) | 3.3V | - (3.3V) | 3.3V | - (1.8V) |
| Vdisp | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 1.8V |
| Vcam | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 1.8V |
| Vio | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 1.8V |
| VETH_VIO_SWITCHED | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 1.8V |
| USB_OTG_VBUS | 5.0V | 5.0V | 5.0V | 5.0V | 5.0V | 5.0V |

Table 1: Voltage groups

3.1 Power supply and reset

3.1.1 Power supply

The DHCOM-iMX6UL(L)-01D2 has the following power connections:

- Vin = Core module supply voltage input
- Vbat = Battery voltage input
- Vsysbus = System bus voltage output
- Vdisp = Display voltage output
- Vcam = Camera voltage output
- VIO = I/O voltage output

Notes to Vbat:

- When no buffer battery is used in the system, Vbat must be connected with 3.3V.
- If you don't have chosen the i.MX6 option [RTC] you can't buffer the date and time information.

Reason: Vbat is only connected to the special temperature compensated RTC RV-8803-C7. The buffering of the included i.MX6 RTC makes no sense, because the current consumption is too high and the buffering range is too small.

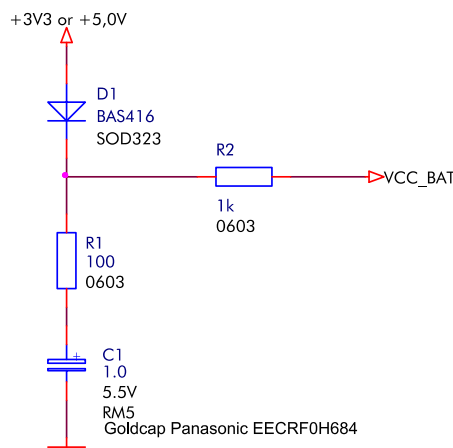


Figure 3: Vbat GoldCap example

The power supply connections Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT are to be used to detect the right voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with the level shifter.

3.1.2 Reset

The System is put in reset state by holding RESET_IN signal low.

When the RESET_IN is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_OUT are asserted as long as RESET_IN is asserted. If the reset input RESET_IN is de-asserted, the RESET_OUT is also de-asserted and the module starts booting again.

3.1.3 Signal Overview

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|-----------------|----------------------------------|-------------------|---------|---------------|----------|
| VCC_IN1 | Core Module supply voltage input | 38 | PWR_I | - | MBC |
| VCC_IN2 | Core Module supply voltage input | 39 | PWR_I | - | MBC |
| VCC_IN3 | Core Module supply voltage input | 40 | PWR_I | - | MBC |
| VCC_IN4 | Core Module supply voltage input | 41 | PWR_I | - | MBC |
| VCC_IN5 | Core Module supply voltage input | 42 | PWR_I | - | MBC |
| VCC_IN6 | Core Module supply voltage input | 44 | PWR_I | - | MBC |
| GND1 | Core Module Ground | 17 | PWR_I | - | MBC |
| GND2 | Core Module Ground | 19 | PWR_I | - | MBC |
| GND3 | Core Module Ground | 43 | PWR_I | - | MBC |
| GND4 | Core Module Ground | 45 | PWR_I | - | MBC |
| GND5 | Core Module Ground | 47 | PWR_I | - | MBC |
| GND6 | Core Module Ground | 101 | PWR_I | - | MBC |
| GND7 | Core Module Ground | 111 | PWR_I | - | MBC |
| GND8 | Core Module Ground | 153 | PWR_I | - | MBC |
| GND9 | Core Module Ground | 185 | PWR_I | - | MBC |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|-----------------|--------------------------------------|-------------------|---------|---------------|----------|
| GND10 | Core Module Ground | 199 | PWR_I | - | MBC |
| VCC_BAT | Core Module Battery voltage input | 200 | PWR_I | - | MBC |
| VDDA_Audio | Audio Codec supply voltage input | 10 | PWR_I | - | MBC |
| VSSA_Audio | Audio Codec Ground | 9 | PWR_I | - | MBC |
| Vsysbus_OUT | System bus supply voltage output | 110 | PWR_0 | - | - |
| Vdisp_OUT | LCD controller supply voltage output | 46 | PWR_0 | - | - |
| Vcam_OUT | Camera supply voltage output | 102 | PWR_0 | - | - |
| VIO_OUT | I/O supply voltage output | 152 | PWR_0 | - | - |
| RESET_IN | System Reset input (active low) | 21 | I | - | - |
| RESET_OUT | System Reset output (active low) | 20 | 0 | - | - |

Table 2: SODIMM-200 Power supply and reset

3.2 Hardware coding

The following pins can be used to read out the current hardware version of the DHCOM i.MX6 core module.

| CPU ball name | Description | CPU ball number | IO Type |
|---------------|-------------|-----------------|---------|
| CSI_DATA00 | Code_HW_0 | E4 | I |
| CSI_DATA01 | Code_HW_1 | E3 | I |
| CSI_DATA02 | Code_HW_2 | E2 | I |

Table 3: Hardware coding

| DH PCB Numbers | Description | Code_HW_2 | Code_HW_1 | Code_HW_0 |
|---------------------------|------------------------|------------|------------|------------|
| 579-100 (current version) | DHCOM-iMX6UL(L)-i-01D2 | 0 (10k PD) | 0 (10k PD) | 0 (10k PD) |
| | | | | |
| ... | | ... | ... | ... |

Table 4: Different hardware versions

3.3 Touch controller

The DHCOM-iMX6UL(L)-01D2 module is equipped with a 4-Wire 12 bit resistive Touch Controller (iMX6ULL integrated peripheral).

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | CPU ball number | Not used |
|-----------------|-------------------------------|-------------------|---------|---------------|-----------------|----------|
| TSPX | Resistive Touch: 4 wire (X +) | 12 | AINOUT | GPI01_I004 | M16 | |
| TSMX | Resistive Touch: 4 wire (X -) | 14 | AINOUT | GPI01_I003 | L17 | |
| TSMY | Resistive Touch: 4 wire (Y -) | 16 | AINOUT | GPI01_I001 | L15 | |
| TSPY | Resistive Touch: 4 wire (Y +) | 18 | AINOUT | GPI01_I002 | L14 | |

Table 5: Touch controller connections

3.4 Ethernet

The DHCM-iMX6UL(L)-01D2 module includes two 10/100 Ethernet controller (Microchip LAN8710Ai). Each controller is connected to a separate EEPROM which contains a MAC address. The two Ethernet interfaces fulfil the IEEE1588 conform standard.

For more precise information, we refer here to the data sheet and other technical documents of Microchip.

<https://www.microchip.com/>

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|------------------|---|-------------------|---------|---------------|----------|
| nETH1_LINK_LED | Port 1: Activity LED connection | 186 | 0 | - | PD |
| nETH1_SPEED_LED | Port 1: Speed LED connection | 188 | 0 | - | PU |
| ETH1_TXD- | Port 1: Ethernet TX Differential Output (minus) | 190 | 0 | - | PD |
| ETH1_TXD+ | Port 1: Ethernet TX Differential Output (plus) | 192 | 0 | - | PD |
| ETH_VIO_SWITCHED | Analogue power supply output to magnetics | 194 | PWR_0 | - | - |
| ETH1_RXI- | Port 1: Ethernet TX Differential Input (minus) | 196 | I | - | PD |
| ETH1_RXI+ | Port 1: Ethernet TX Differential Input (plus) | 198 | I | - | PD |
| | | | | | |
| nETH2_LINK_LED | Port 2: Activity LED connection | 187 | 0 | - | PD |
| nETH2_SPEED_LED | Port 2: Speed LED connection | 189 | 0 | - | PU |
| ETH2_TXD- | Port 2: Ethernet TX Differential Output (minus) | 191 | 0 | - | PD |
| ETH2_TXD+ | Port 2: Ethernet TX Differential Output (plus) | 193 | 0 | - | PD |
| ETH2_RXI- | Port 2: Ethernet TX Differential Input (minus) | 195 | I | - | PD |
| ETH2_RXI+ | Port 2: Ethernet TX Differential Input (plus) | 197 | I | - | PD |

Table 6: Ethernet connections

Note: The LED outputs “nETH*_LINK_LED” and “nETH*_SPEED_LED” must be connected as follows:

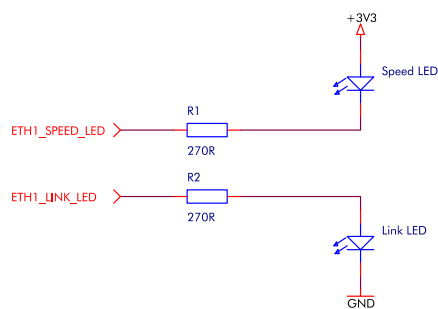


Figure 4: Ethernet LED circuitry

Note: In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration lines.

Note: Ethernet 2 interface can only be used if SPI 2 interface is not used.

3.5 USB

The DHCM-iMX6UL(L)-01D2 module supports a maximum of two USB devices. These consist of one USB OTG connection and one USB host connection. For both connections the integrated iMX6ULL PHYs are used.

All two ports are high-speed USB connections, which also support full speed and low speed.

3.5.1 USB OTG

This USB interface fulfils the USB 2.0 specification. It can be configured as OTG, host or device and supports all speeds.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Not used |
|-----------------|---|-------------------|----------------|-----------------|---------------|----------|
| USB_OTG_VBUS | OTG Client: VBUS Input line OTG Host: USB bus supply voltage | 166 | I PWR_0 | T12 | USB_OTG1_VBUS | PD |
| USB_OTG_ID | OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client) | 168 | I | K13 | GPIO1_I000 | - |
| USB_OTG_D+ | USB OTG differential Signal positive line | 170 | IO | U15 | USB_OTG1_DP | PD |
| USB_OTG_D- | USB OTG differential Signal negative line | 172 | IO | T15 | USB_OTG1_DN | PD |

Table 7: USB OTG

Note: The DHCOM USB OTG port does not provide any “enable” and “over current” signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event, the “over current” output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

3.5.2 USB Host

The USB Host 1 port fulfils the USB 2.0 specification. It supports high-speed, full speed and low speed data transfers.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Not used |
|-----------------|--|-------------------|---------|------------------------|--|----------|
| USB_PWR_STAT | USB Host over current indicator (active low) | 174 | I | On request: L17 | On request: GPIO1_I003 | - |
| USB_PWR_EN | USB Host power enable signal (active low) | 176 | 0 | M17 On request: L14 | On request: GPIO1_I005 On request: GPIO1_I002 | - |
| USB_HOST_D1+ | USB Host differential Signal positive line | 178 | IO | U13 | USB_OTG2_DP | PD |
| USB_HOST_D1- | USB Host differential Signal negative line | 180 | IO | T13 | USB_OTG2_DN | PD |

Table 8: USB Host

Note: USB_PWR_EN signal connection depends on variant. USB_PWR_STAT is not connected at default variant.

3.6 UART

The DHCM-iMX6UL(L)-01D2 module offers connections for a total of two UARTs. UART 1 and UART 2 additionally support a hardware handshake.

The maximum transfer rate is 5 Mbit/s.

For more precise information, we refer here to the data sheet and other technical documents of NXP:

<http://www.nxp.com/>

3.6.1 UART 1

Note: DHCOM UART 1 is the UART 1 module of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Not used |
|-----------------|-------------------------|-------------------|---------|-----------------|---------------|----------|
| UART1_CTS | UART clear to send | 24 | I | J14 | UART1_RTS_B | - |
| UART1_RTS | UART request to send | 26 | O | K15 | UART1_CTS_B | - |
| UART1_RX | UART receive data line | 32 | I | K16 | UART1_RX_DATA | - |
| UART1_TX | UART transmit data line | 34 | O | K14 | UART1_TX_DATA | - |

Table 9: UART 1

Hardware design notes: It is essential to always create a possible connection to DHCOM UART 1, since the DHCOM bootloader can be operated with the UART 1. A minimum connection possibility should be made available via solder pads.

Note: UART CTS and RTS signals are only available if CAN port 2 is not available. This means a module variant without option –CAN2 must be used to support hardware handshake.

3.6.2 UART 2

Note: DHCOM UART 2 is the UART 2 module of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Not used |
|-----------------|-------------------------|-------------------|---------|-----------------|---------------|----------|
| UART2_CTS | UART clear to send | 31 | I | H16 | UART3_RX_DATA | - |
| UART2_RTS | UART request to send | 33 | O | H17 | UART3_TX_DATA | - |
| UART2_RX | UART receive data line | 35 | I | J16 | UART2_RX_DATA | - |
| UART2_TX | UART transmit data line | 37 | O | J17 | UART2_TX_DATA | - |

Table 10: UART 2

3.7 Serial port interface

The DHCM-iMX6UL(L)-01D2 module is equipped with two SPI interfaces. These interfaces consist of a full duplex capable, 4-wire interface and have the following characteristics:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers

- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

For more precise information, we refer here to the data sheet and other technical documents of NXP:

<http://www.nxp.com/>

3.7.1 SPI 1

Notes:

- DHCOM SPI Port 1 is connected to the ECSP1 interface of the iMX6ULL
- The ECSP1 interface of the iMX6ULL is also used for the onboard SPI flash
- ECSP1 interface is shared with CSI interface during access to onboard SPI Boot Flash
- ECSP1 interface is shared with LCD interface during normal run time. LCD functionality is not affected because of 18bit color depth (shared pins are Bit20...Bit23). That means LCD end external SPI 1 interface can simultaneously be used.
- SPI1_CS0 on the SODIMM-200 socket uses the ECSP1_SS0 signal of the iMX6ULL
- ECSP1_SS0 is used for the on-board SPI flash (in combination with signal SPI_BOOT_FLASH_EN, which is connected to cpu ball GPIO1_I009)

3.7.1.1 SPI 1 during boot time (booting from onboard SPI Flash)

| SPI Flash signals | Description | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|--------------------------|---|---------|-----------------|---------------|--------------------|----------|
| SPI Flash CS | Slave select signal (Or'ed with GPIO1_I009) | 0 | D3 | CSI_DATA05 | ECSP1_SS0 | - |
| SPI Flash CLK | clock line | 0 | D4 | CSI_DATA04 | ECSP1_SCLK | - |
| SPI Flash MISO | receive data line | I | D1 | CSI_DATA07 | ECSP1_MISO | - |
| SPI Flash MOSI | transmit data line | 0 | D2 | CSI_DATA06 | ECSP1_MOSI | - |
| Signal SPI_BOOT_FLASH_EN | Must be set 0 to activate onboard SPI Flash | 0 | M15 | GPIO1_I009 | | |

Table 11: SPI1 Interface during boot time

3.7.1.2 SPI 1 during Linux run time (no access to onboard SPI Flash)

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|---|-------------------|---------|-----------------|---------------|--------------------|----------|
| SPI1_CS0 | Slave select signal | 177 | 0 | B14 | LCD_DATA21 | ECSP1_SS0 | - |
| SPI1_CLK | SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation) | 179 | IO | C14 | LCD_DATA20 | ECSP1_SCLK | - |
| SPI1_MISO | SSP receive data line | 181 | I | B16 | LCD_DATA23 | ECSP1_MISO | - |
| SPI1_MOSI | SSP transmit data line | 183 | 0 | A14 | LCD_DATA22 | ECSP1_MOSI | - |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------------------|---|-------------------|---------|-----------------|---------------|--------------------|----------|
| Signal SPI_BOOT_FLASH_EN | Must be set 1 to deactivate onboard SPI Flash | | 0 | M15 | GPIO1_I009 | | |

Table 12: SPI1 Interface during run time

3.7.1.3 SPI 1 function overview

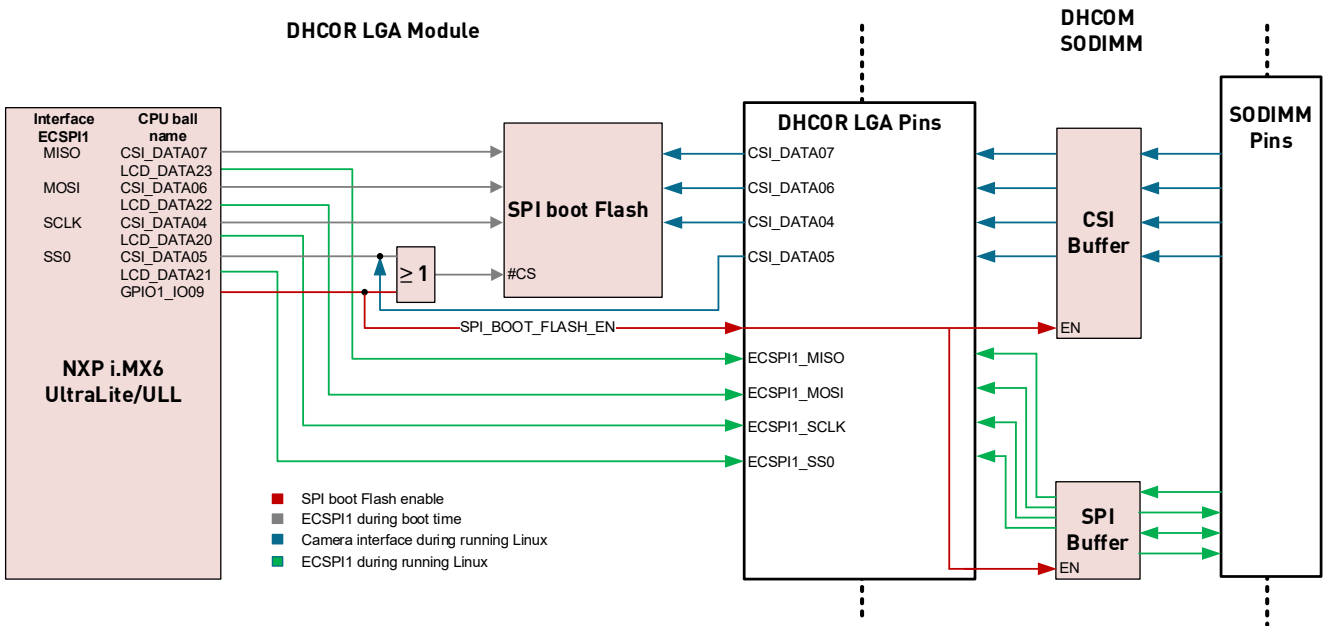


Figure 5: SPI 1 Function Overview

Because of the lack of available pins of the iMX6ULL, the two different ECSP1 interfaces have to be shared with LCD interface and CSI interface. The following table describes how to use these interfaces.

| Interface | SPI CS to be used | SPI_BOOT_FLASH_EN (GPIO1_I009) | Note |
|--------------------------|-------------------------|--|--|
| CSI | | Must be set 1 to enable external CSI buffer | Onboard SPI Flash cannot be accessed. |
| LCD | | Do not care | External SPI 1 can simultaneously be used. |
| External SPI 1 | LCD_DATA21 (ECSP11_SS0) | Must be set 1 to enable external SPI buffer | 18 bit LCD can simultaneously be used. |
| Onboard SPI (Boot Flash) | CSI_DATA05 (ECSP11_SS0) | Must be set 0 to disable external CSI buffer. Signal is Or'ed with CSI_DATA05 (ECSP11_SS0) | - |

Table 13: CSI, LCD, SPI function matrix

Note: LCD Pins are Boot Config Pins, therefore it must be ensured that during boot time signal SPI_BOOT_FLASH_EN (GPIO1_I009) is set 0, to disable external SPI buffer.

3.7.2 SPI 2

Notes:

- DHCOM SPI Port 2 is connected to the ECSPi4 interface of the i.MX6ULL
- SPI2_CS0 on the SODIMM-200 socket uses the ECSPi4_SS0 signal of the i.MX6ULL
- DHCOM SPI Port 2 can only be used if Ethernet 2 is not used. This means that DHCOM SPI Port 2 is only available if a variant without dual Ethernet option –E2 is used.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|---|-------------------|---------|-----------------|----------------|--------------------|----------|
| SPI2_CS0 | Slave select signal | 155 | 0 | D16 | ENET2_RX_ER | ECSPi4_SS0 | - |
| SPI2_CLK | SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation) | 157 | IO | A16 | ENET2_TX_DATA1 | ECSPi4_SCLK | - |
| SPI2_MISO | SSP receive data line | 159 | I | D17 | ENET2_TX_CLK | ECSPi4_MISO | - |
| SPI2_MOSI | SSP transmit data line | 161 | O | B15 | ENET2_TX_EN | ECSPi4_MOSI | - |

Table 14: SPI 2 Interface

3.8 I²C™

The DHCOM-iMX6UL(L)-01D2 module provides the opportunity to connect up to two separate I²C™ multimaster buses. The I²C™ bus controller integrated in the iMX6ULL has the following main features:

- Compatibility with I2C bus standard
- Multiple-master operation
- Software-programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

Note: The pull-up resistors required according to the I²C™ specification are already fitted on the module. For detailed information about I²C™, reference is made to the specification (Philips Semiconductor):

<http://www.nxp.com>

3.8.1 I2C 1

Note: DHCOM I2C1 uses the I2C2 instance of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|----------------|-------------------|---------|-----------------|---------------|--------------------|----------|
| I2C1_CLK | I2C clock line | 182 | IO | F17 | UART5_TX_DATA | I2C2_SCL | - |
| I2C1_DATA | I2C data line | 184 | IO | G13 | UART5_RX_DATA | I2C2_SDA | - |

Table 15: DHCOM I2C1

3.8.2 I2C 2

Note: DHCOM I2C2 uses the I2C1 instance of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|----------------|-------------------|---------|-----------------|---------------|--------------------|----------|
| I2C1_CLK | I2C clock line | 158 | IO | G17 | UART4_TX_DATA | I2C1_SCL | - |
| I2C1_DATA | I2C data line | 160 | IO | G16 | UART4_RX_DATA | I2C1_SDA | - |

Table 16: DHCOM I2C2

Note: DHCOM I2C2 is also connected to several devices onboard:

| Location | Device | Address |
|----------|----------------------------|---|
| DHCOM | PMIC | Dialog Semiconductor DA-9061 0x58 and 0x59 |
| SODIMM | RTC | Microcrystal RV-8803-C7 0x32 |
| SODIMM | EEProm Ethernet 1 | Microchip 24AA025E48T 0x50 |
| SODIMM | EEProm Ethernet 2 | Microchip 24AA025E48T 0x53 |
| SODIMM | Analog/Digital Converter 1 | Texas Instruments ADC101C027 0x51 |
| SODIMM | Analog/Digital Converter 2 | Texas Instruments ADC101C027 0x52 |

3.9 CAN

The iMX6ULL processor has an integrated standard resp. high-end CAN controller with the following characteristics:

- Supports CAN protocol version 2.0B
- Standard data and remote frames
- Extended data and remote frames
- Zero to eight bytes data length
- Programmable bit rate up to 1 Mb/sec
- Content-related addressing
- Flexible Mailboxes of eight bytes data length
- Each Mailbox is configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Mailbox
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling

- Transmission abort capability
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128
- 100% backwards compatibility with previous FLEXCAN version

3.9.1 CAN 1

Note: DHCOM CAN 1 uses the FLEXCAN1 instance of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|------------------------|-------------------|---------|-----------------|---------------|--------------------|----------|
| CAN_TX | CAN transmit data line | 27 | 0 | H15 | UART3_CTS_B | CAN1_TX | - |
| CAN_RX | CAN receive data line | 29 | I | G14 | UART3_RTS_B | CAN1_RX | - |

Table 17: CAN 1 Interface

3.9.2 CAN 2

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|------------------------|-------------------|---------|-----------------|---------------|--------------------|----------|
| CAN2_TX | CAN transmit data line | 24 | 0 | J15 | UART2_CTS_B | CAN2_TX | - |
| CAN2_RX | CAN receive data line | 26 | I | H14 | UART2_RTS_B | CAN2_RX | - |

Table 18: CAN 2 Interface

Note: DHCOM CAN 2 is only available if option –CAN2 is selected in the specific variant. Then DHCOM UART1 hardware handshake (RTS and CTS) is not available.

3.10 Audio Interface

The DHCM-iMX6UL(L)-01D2 module is equipped with one I2S interface for audio codec connection. This interface has the following characteristics:

- Support for I2S master and slave mode
- Maximum audio sampling rate of 196kHz
- Compliant to Inter-IC Sound (I2S) bus specification from Philips

For more precise information, we refer here to the data sheet and other technical documents of NXP:

<http://www.nxp.com/>

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|----------------------------|-------------------|---------|-----------------|---------------|--------------------|----------|
| I2S_RXD | Data receive signal | 5 | I | M14 | JTAG_TCK | SAI2_RX_DATA | PD |
| I2S_TXFS | Transmit Frame sync signal | 11 | 0 | N15 | JTAG_TDO | SAI2_TX_SYNC | - |
| I2S_TXD | Data transmit signal | 15 | 0 | N14 | JTAG_TRST_B | SAI2_TX_DATA | - |
| I2S_TXC | Transmit clock signal | 13 | 0 | N16 | JTAG_TDI | SAI2_TX_BCLK | - |

Table 19: Audio Interface

Note: The I2S lines are shared with JTAG!

3.11 Display

3.11.1 RGB

The DHCM-iMX6UL(L)-01D2 module enables the connection of a 18 bit LCD display. Active as well as passive LCD displays with a resolution of up to 1366 x 768 pixels can be operated.

The core of the LCD controller is the Enhanced LCD Interface (eLCDIF) in the iMX6ULL. More precise information about this is available in the iMX6ULL Reference Manual:

<http://www.nxp.com/>

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Boot Config Pin / Mux func. name | Not used |
|-----------------|--------------------------------------|-------------------|---------|-----------------|---------------|----------------------------------|----------|
| Vdisp_OUT | LCD controller supply voltage output | 46 | PWR_0 | --- | --- | --- | (*) |
| LC_R0 | LCD display data red 0 | 76 | 0 | --- | --- | --- | (*) |
| LC_R1 | LCD display data red 1 | 78 | 0 | --- | --- | --- | (*) |
| LC_R2 | LCD display data red 2 | 49 | 0 | C12 | LCD_DATA12 | BT_CFG2[4] | (*) |
| LC_R3 | LCD display data red 3 | 51 | 0 | B12 | LCD_DATA13 | BT_CFG2[5] | (*) |
| LC_R4 | LCD display data red 4 | 53 | 0 | A12 | LCD_DATA14 | BT_CFG2[6] | (*) |
| LC_R5 | LCD display data red 5 | 55 | 0 | D13 | LCD_DATA15 | BT_CFG2[7] | (*) |
| LC_R6 | LCD display data red 6 | 57 | 0 | C13 | LCD_DATA16 | BT_CFG4[0] | (*) |
| LC_R7 | LCD display data red 7 | 59 | 0 | B13 | LCD_DATA17 | BT_CFG4[1] | (*) |
| LC_G0 | LCD display data green 0 | 80 | 0 | --- | --- | --- | (*) |
| LC_G1 | LCD display data green 1 | 82 | 0 | --- | --- | --- | (*) |
| LC_G2 | LCD display data green 2 | 61 | 0 | A10 | LCD_DATA06 | BT_CFG1[6] | (*) |
| LC_G3 | LCD display data green 3 | 63 | 0 | D11 | LCD_DATA07 | BT_CFG1[7] | (*) |
| LC_G4 | LCD display data green 4 | 65 | 0 | B11 | LCD_DATA08 | BT_CFG2[0] | (*) |
| LC_G5 | LCD display data green 5 | 67 | 0 | A11 | LCD_DATA09 | BT_CFG2[1] | (*) |
| LC_G6 | LCD display data green 6 | 69 | 0 | E12 | LCD_DATA10 | BT_CFG2[2] | (*) |
| LC_G7 | LCD display data green 7 | 71 | 0 | D12 | LCD_DATA11 | BT_CFG2[3] | (*) |
| LC_B0 | LCD display data blue 0 | 84 | 0 | --- | --- | --- | (*) |
| LC_B1 | LCD display data blue 1 | 86 | 0 | --- | --- | --- | (*) |
| LC_B2 | LCD display data blue 2 | 73 | 0 | B9 | LCD_DATA00 | BT_CFG1[0] | (*) |
| LC_B3 | LCD display data blue 3 | 75 | 0 | A9 | LCD_DATA01 | BT_CFG1[1] | (*) |
| LC_B4 | LCD display data blue 4 | 77 | 0 | E10 | LCD_DATA02 | BT_CFG1[2] | (*) |
| LC_B5 | LCD display data blue 5 | 79 | 0 | D10 | LCD_DATA03 | BT_CFG1[3] | (*) |
| LC_B6 | LCD display data blue 6 | 81 | 0 | C10 | LCD_DATA04 | BT_CFG1[4] | (*) |
| LC_B7 | LCD display data blue 7 | 83 | 0 | B10 | LCD_DATA05 | BT_CFG1[5] | (*) |
| LC_EN | LCD display data enable | 85 | 0 | B8 | LCD_ENABLE | | (*) |
| LC_VSYNC | LCD frame or vertical sync. puls | 87 | 0 | C9 | LCD_VSYNC | | (*) |
| LC_HSYNC | LCD line or horizontal sync. puls | 89 | 0 | D9 | LCD_HSYNC | | (*) |
| LC_PCLK | LCD pixel clock | 91 | 0 | A8 | LCD_CLK | | (*) |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | Boot Config Pin / Mux func. name | Not used |
|-----------------|--|-------------------|---------|-----------------|---------------|----------------------------------|----------|
| GPI0_PWM | LCD contrast (only if PWM is not used) | 100 | 0 | N17 | GPI01_I008 | PWM1_OUT | (*) |

Table 20: RGB Interface

Note: (*) Regarding EMC it is recommended to terminate RGB interface lines with PD resistor.

Note: LCD Datapins are shared with Boot Configuration Pins. If boot configuration is saved to efuses, then the condition of the pins does not matter during start-up.

3.12 Boot Mode

The default configuration of the Boot Mode is “Internal Boot”. This means the boot configuration pins are sampled at power up. With a specific bootloader command the configuration can be programmed to the eFuses. In all further boot processes the eFuses are read at power up instead of the Boot config pins. The default boot device is SPI flash. If the flash gets corrupt or erased by mistake, a small tactile switch can be used to start-up with “Serial Downloader” boot mode. This switch will only be available in development variants of the DHCOM module.

3.13 PWM

The DHCM-iMX6UL(L)-01D2 module enables the connection to Pulse Width Modulation (PWM) output.

More precise information about this is available in the iMX6ULL Reference Manual:

<http://www.nxp.com/>

Note: DHCOM PWM uses the pwm1 instance of the iMX6ULL.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|--|-------------------|---------|-----------------|---------------|--------------------|----------|
| GPI0_PWM | PWM channel (only if LCD contrast is not used) | 100 | 0 | N17 | GPI01_I008 | PWM1_OUT | - |

Table 21: PWM Interface

3.14 SD/MMC/SDIO controller

The iMX6ULL processor has a SD/MMC/SDIO card host controller integrated. There is only one controller to access the on-board microSD card or a SD/MMC/SDIO interface to the SODIMM-200 socket.

Note: DHCOM MMC/SD is only available if microSD socket and WiFi is not mounted (module variant without option –WBT and –SD). Also on module microSD socket is only available if WiFi (module variant without option –WBT) is not mounted.

Main characteristics:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5
- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the SDIO Card Specification version 3.0
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit MMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes

3.14.1 On-board microSD socket

| Signal name | Description | uSD socket pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-------------|---|-----------------------|---------|-----------------|---------------|--------------------|----------|
| SD_CLK | SD/SDIO/MMC bus clock | 5 | 0 | C1 | SD1_CLK | | - |
| SD_CMD | SD/SDIO/MMC command line | 3 | IO | C2 | SD1_CMD | | - |
| SD_DETECT | SD/SDIO/MMC card detection (LOW when card inserted) | G3 | I | J14 | UART1_RTS_B | GPI01_I019 | - |
| SD_D0 | SD/SDIO/MMC data line | 7 | IO | B3 | SD1_DATA0 | | - |
| SD_D1 | SD/SDIO/MMC data line | 8 | IO | B2 | SD1_DATA1 | | - |
| SD_D2 | SD/SDIO/MMC data line | 1 | IO | B1 | SD1_DATA2 | | - |
| SD_D3 | SD/SDIO/MMC data line | 2 | IO | A2 | SD1_DATA3 | | - |

Table 22: On-board microSD card socket

3.14.2 SD/MMC/SDIO interface

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Not used |
|-----------------|--|-------------------|---------|-----------------|---------------|--------------------|----------|
| SD_CLK | SD/SDIO/MMC bus clock | 103 | 0 | C1 | SD1_CLK | | - |
| SD_CMD | SD/SDIO/MMC command line | 104 | IO | C2 | SD1_CMD | | - |
| SD_DETECT | SD/SDIO/MMC card detection (active high) | 105 | I | J14 | UART1_RTS_B | GPI01_I019 | PU |
| SD_D0 | SD/SDIO/MMC data line | 106 | IO | B3 | SD1_DATA0 | | - |
| SD_D1 | SD/SDIO/MMC data line | 107 | IO | B2 | SD1_DATA1 | | - |
| SD_D2 | SD/SDIO/MMC data line | 108 | IO | B1 | SD1_DATA2 | | - |
| SD_D3 | SD/SDIO/MMC data line | 109 | IO | A2 | SD1_DATA3 | | - |

Table 23: SD/MMC/SDIO Interface

3.15 GPIOs

The DHCM-iMX6UL(L)-01D2 module provides several GPIO pins on the SODIMM-200 socket.

Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHCOM standard.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | CPU ball name | CPU mux func. name | Out of reset state | Not used |
|---------------------------------|---|-------------------|---------|-----------------|---------------|--------------------|--------------------|----------|
| INT_HIGHEST_PRIORITY | Highest priority interrupt pin (active low) | 151 | IO | P14 | JTAG_TMS | GPIO1_I011 | In / 47k PU | PU |
| GPIO_A | General Purpose I/O | 154 | IO | R10 | SNVS_TAMPER0 | GPIO5_I000 | In / Keeper | - |
| GPIO_B | General Purpose I/O | 156 | IO | R9 | SNVS_TAMPER1 | GPIO5_I001 | In / Keeper | - |
| GPIO_C | General Purpose I/O | 162 | IO | P11 | SNVS_TAMPER2 | GPIO5_I002 | In / Keeper | - |
| GPIO_D | General Purpose I/O | 163 | IO | P10 | SNVS_TAMPER3 | GPIO5_I003 | In / Keeper | - |
| GPIO_E | General Purpose I/O | 164 | IO | P9 | SNVS_TAMPER4 | GPIO5_I004 | In / Keeper | - |
| GPIO_F | General Purpose I/O | 165 | IO | N10 | SNVS_TAMPER7 | GPIO5_I007 | In / Keeper | - |
| GPIO_G | General Purpose I/O | 167 | IO | N9 | SNVS_TAMPER8 | GPIO5_I008 | In / Keeper | - |
| GPIO_H | General Purpose I/O | 173 | IO | R6 | SNVS_TAMPER9 | GPIO5_I009 | In / Keeper | - |
| GPIO_I | General Purpose I/O | 175 | IO | K15 | UART1_CTS_B | GPIO1_I018 | In / Keeper | - |
| VIO_OUT | Voltage for external Level-Shifter | 152 | PWR_0 | | | | | |
| GPIO_J (or CIF_HSYNC) | General Purpose I/O | 74 | IO | F3 | CSI_HSYNC | GPIO4_I020 | In / Keeper | - |
| GPIO_K (or CIF_PCLK) | General Purpose I/O | 72 | IO | E5 | CSI_PIXCLK | GPIO4_I018 | In / Keeper | - |
| GPIO_L (or CIF_MCLK) | General Purpose I/O | 70 | IO | F5 | CSI_MCLK | GPIO4_I017 | In / Keeper | - |
| GPIO_M (or CIF_VSYNC) | General Purpose I/O | 68 | IO | F2 | CSI_VSYNC | GPIO4_I019 | In / Keeper | - |
| GPIO_N (or CIF_D9) ⁵ | General Purpose I/O | 66 | IO | D1 | CSI_DATA07 | GPIO4_I028 | In / Keeper | - |
| GPIO_O (or CIF_D8) ⁵ | General Purpose I/O | 64 | IO | D2 | CSI_DATA06 | GPIO4_I027 | In / Keeper | - |
| GPIO_P (or CIF_D7) ⁵ | General Purpose I/O | 62 | IO | D3 | CSI_DATA05 | GPIO4_I026 | In / Keeper | - |
| GPIO_Q (or CIF_D6) ⁵ | General Purpose I/O | 60 | IO | D4 | CSI_DATA04 | GPIO4_I025 | In / Keeper | - |
| GPIO_R (or CIF_D5) ⁵ | General Purpose I/O | 58 | IO | E1 | CSI_DATA03 | GPIO4_I024 | In / Keeper | - |
| GPIO_S (or CIF_D4) ⁵ | General Purpose I/O | 56 | IO | E2 | CSI_DATA02 | GPIO4_I023 | In / Keeper | - |
| GPIO_T (or CIF_D3) ⁵ | General Purpose I/O | 54 | IO | E3 | CSI_DATA01 | GPIO4_I022 | In / Keeper | - |
| GPIO_U (or CIF_D2) ⁵ | General Purpose I/O | 52 | IO | E4 | CSI_DATA00 | GPIO4_I021 | In / Keeper | - |
| GPIO_V (or CIF_D1) | General Purpose I/O | 50 | IO | - | - | - | - | - |
| GPIO_W (or CIF_D0) | General Purpose I/O | 48 | IO | - | - | - | - | - |
| Vcam_OUT | Voltage for external Level-Shifter | 102 | PWR_0 | | | | | |

Table 24: GPIO pin assignment

Note: The GPIOs of the iMX6ULL can only drive at a maximum of roughly 2mA (depends on the pad drive strength). Where a greater current is required, an additional driver must be provided on the carrier board. The minimum and maximum logic level can be obtained from the data sheet of the iMX6ULL.

<http://www.nxp.com/>

⁵ Pins are buffered via TI TXS0108EPWR between CPU and SODIMM connector.

3.16 Analog Inputs

The DHCM-iMX6UL(L)-01D2 module provides two analog input pins on the SODIMM-200 socket. For each channel an analog to digital converter with I2C interface is used (ADC101C027).

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball number | Range | I2C Addr | Not used |
|-----------------|------------------------|-------------------|---------|-----------------|--------|----------|----------|
| AD0_IN | Analog input channel 0 | 8 | I | - | 0-3.3V | 0x51 | - |
| AD1_IN | Analog input channel 1 | 6 | I | - | 0-3.3V | 0x52 | - |

Table 25: Analog inputs

3.17 WiFi / Bluetooth

The DHCM-iMX6UL(L)-01D2 system-on-module provides a 2.4GHz wireless local area network (WLAN) and Bluetooth (BT) solution via the Murata 1DX module. Based on Cypress CYW4343W, the module provide high-efficiency RF front end circuits. The module is designed to fit into small spaces.

- **WiFi:** IEEE802.11b/g/n W-LAN
- **Bluetooth:** Bluetooth® v5.1 (BR/EDR/BLE)

The module has one antenna port, via a dedicated U.FL connector.

4 Plugs and connections

Additionally to the SODIMM-200 connector, the DHCM-iMX6UL(L)-01D2 module is equipped with a 10pin FFC and Tag-Connect JTAG connector, a separate microSD card socket and the U.FL WiFi / Bluetooth antenna connector.

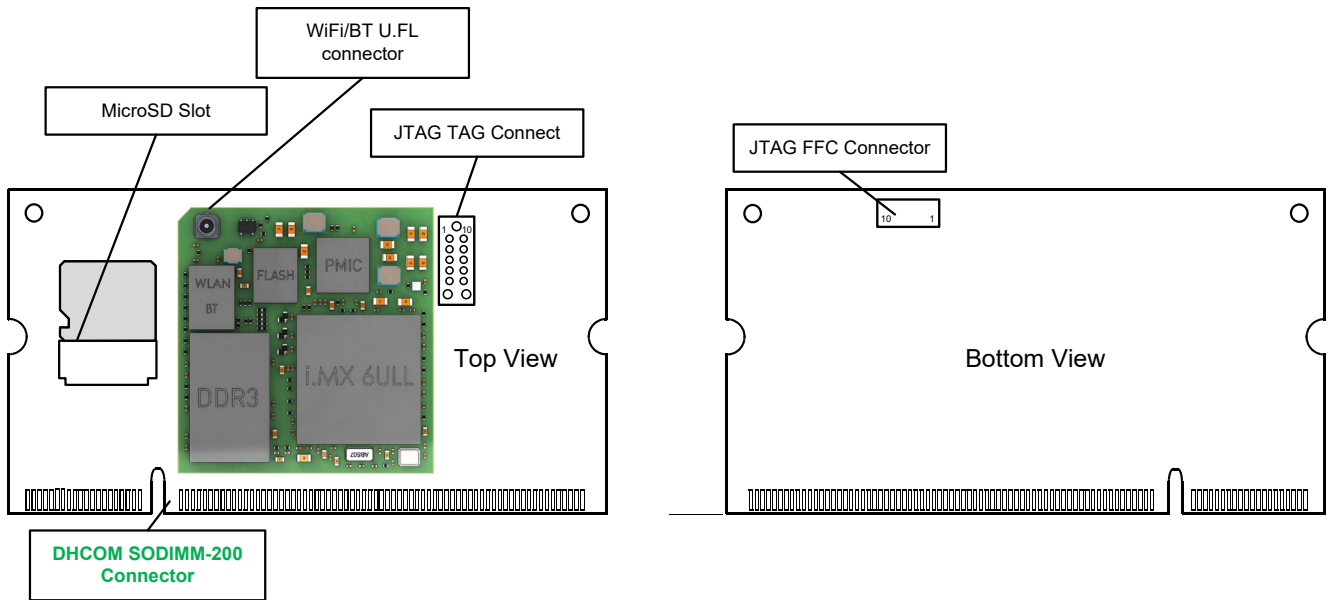


Figure 6: Position of the plugs and connections

4.1 SODIMM-200

| Pin number | Pin name | Power domain |
|------------|-----------------|--------------|
| 1 | <i>Reserved</i> | VDDA |
| 3 | <i>Reserved</i> | VDDA |
| 5 | I2S_RXD | VIO |
| 7 | <i>Reserved</i> | VDDA |
| 9 | <i>Reserved</i> | VDDA |
| 11 | I2S_TXFS | VIO |
| 13 | I2S_TXC | VIO |
| 15 | I2S_TXD | VIO |
| 17 | GND1 | Vin |
| 19 | GND2 | Vin |
| 21 | RESET_IN | VIO |
| 23 | <i>Reserved</i> | VIO |
| 25 | <i>Reserved</i> | VIO |
| 27 | CAN_TX | VIO |
| 29 | CAN_RX | VIO |
| 31 | UART2_CTS | VIO |
| 33 | UART2_RTS | VIO |
| 35 | UART2_RX | VIO |
| 37 | UART2_TX | VIO |
| 39 | VCC_IN2 | Vin |
| 41 | VCC_IN4 | Vin |
| 43 | GND3 | Vin |
| 45 | GND4 | Vin |
| 47 | GND5 | Vin |
| 49 | LC_R2 | Vdisp |
| 51 | LC_R3 | Vdisp |
| 53 | LC_R4 | Vdisp |
| 55 | LC_R5 | Vdisp |
| 57 | LC_R6 | Vdisp |
| 59 | LC_R7 | Vdisp |
| 61 | LC_G2 | Vdisp |
| 63 | LC_G3 | Vdisp |
| 65 | LC_G4 | Vdisp |
| 67 | LC_G5 | Vdisp |
| 69 | LC_G6 | Vdisp |
| 71 | LC_G7 | Vdisp |
| 73 | LC_B2 | Vdisp |
| 75 | LC_B3 | Vdisp |
| 77 | LC_B4 | Vdisp |
| 79 | LC_B5 | Vdisp |
| 81 | LC_B6 | Vdisp |
| 83 | LC_B7 | Vdisp |
| 85 | LC_EN | Vdisp |
| 87 | LC_VSYNC | Vdisp |

| Pin number | Pin name | Power domain |
|------------|-----------------------|--------------|
| 2 | <i>Reserved</i> | VDDA |
| 4 | <i>Reserved</i> | VDDA |
| 6 | Analog Input 1 | VDDA |
| 8 | Analog Input 0 | VDDA |
| 10 | <i>Reserved</i> | VDDA |
| 12 | TSPX | VDDA |
| 14 | TSMX | VDDA |
| 16 | TSMY | VDDA |
| 18 | TSPY | VDDA |
| 20 | RESET_OUT | VIO |
| 22 | <i>Reserved</i> | VIO |
| 24 | UART1_CTS or CAN2_TX | VIO |
| 26 | UART1_RTS or CAN2_RX | VIO |
| 28 | <i>Reserved</i> | VIO |
| 30 | <i>Reserved</i> | VIO |
| 32 | UART1_RX | VIO |
| 34 | UART1_TX | VIO |
| 36 | <i>Reserved</i> | VIO |
| 38 | VCC_IN1 | Vin |
| 40 | VCC_IN3 | Vin |
| 42 | VCC_IN5 | Vin |
| 44 | VCC_IN6 | Vin |
| 46 | Vdisp_OUT | Vdisp |
| 48 | <i>Reserved</i> | Vcam |
| 50 | <i>Reserved</i> | Vcam |
| 52 | GPIO_U (or CIF_D2) | Vcam |
| 54 | GPIO_T (or CIF_D3) | Vcam |
| 56 | GPIO_S (or CIF_D4) | Vcam |
| 58 | GPIO_R (or CIF_D5) | Vcam |
| 60 | GPIO_Q (or CIF_D6) | Vcam |
| 62 | GPIO_P (or CIF_D7) | Vcam |
| 64 | GPIO_O (or CIF_D8) | Vcam |
| 66 | GPIO_N (or CIF_D9) | Vcam |
| 68 | GPIO_M (or CIF_VSYNC) | Vcam |
| 70 | GPIO_L (or CIF_MCLK) | Vcam |
| 72 | GPIO_K (or CIF_PCLK) | Vcam |
| 74 | GPIO_J (or CIF_HSYNC) | Vcam |
| 76 | <i>Reserved</i> | Vdisp |
| 78 | <i>Reserved</i> | Vdisp |
| 80 | <i>Reserved</i> | Vdisp |
| 82 | <i>Reserved</i> | Vdisp |
| 84 | <i>Reserved</i> | Vdisp |
| 86 | <i>Reserved</i> | Vdisp |
| 88 | <i>Reserved</i> | LVDS |

| Pin number | Pin name | Power domain |
|------------|----------------------|--------------|
| 89 | LC_HSYNC | Vdisp |
| 91 | LC_PCLK | Vdisp |
| 93 | <i>Reserved</i> | LVDS |
| 95 | <i>Reserved</i> | LVDS |
| 97 | <i>Reserved</i> | LVDS |
| 99 | <i>Reserved</i> | LVDS |
| 101 | GND6 | Vin |
| 103 | SD_CLK | VIO |
| 105 | SD_DETECT | VIO |
| 107 | SD_D1 | VIO |
| 109 | SD_D3 | VIO |
| 111 | GND7 | Vin |
| 113 | <i>Reserved</i> | Vsysbus |
| 115 | <i>Reserved</i> | Vsysbus |
| 117 | <i>Reserved</i> | Vsysbus |
| 119 | <i>Reserved</i> | Vsysbus |
| 121 | <i>Reserved</i> | Vsysbus |
| 123 | <i>Reserved</i> | Vsysbus |
| 125 | <i>Reserved</i> | Vsysbus |
| 127 | <i>Reserved</i> | Vsysbus |
| 129 | <i>Reserved</i> | Vsysbus |
| 131 | <i>Reserved</i> | Vsysbus |
| 133 | <i>Reserved</i> | Vsysbus |
| 135 | <i>Reserved</i> | Vsysbus |
| 137 | <i>Reserved</i> | Vsysbus |
| 139 | <i>Reserved</i> | Vsysbus |
| 141 | <i>Reserved</i> | Vsysbus |
| 143 | <i>Reserved</i> | Vsysbus |
| 145 | <i>Reserved</i> | Vsysbus |
| 147 | <i>Reserved</i> | Vsysbus |
| 149 | <i>Reserved</i> | Vsysbus |
| 151 | INT_HIGHEST_PRIORITY | VIO |
| 153 | GND8 | Vin |
| 155 | SPI2_CS0 | VIO |
| 157 | SPI2_CLK | VIO |
| 159 | SPI2_MISO | VIO |
| 161 | SPI2_MOSI | VIO |
| 163 | GPIO_D | VIO |
| 165 | GPIO_F | VIO |
| 167 | GPIO_G | VIO |
| 169 | <i>Reserved</i> | USB |
| 171 | <i>Reserved</i> | USB |
| 173 | GPIO_H | VIO |
| 175 | GPIO_I | VIO |
| 177 | SPI1_CS0 | VIO |
| 179 | SPI1_CLK | VIO |
| 181 | SPI1_MISO | VIO |

| Pin number | Pin name | Power domain |
|------------|-----------------|--------------|
| 90 | <i>Reserved</i> | LVDS |
| 92 | <i>Reserved</i> | LVDS |
| 94 | <i>Reserved</i> | LVDS |
| 96 | <i>Reserved</i> | LVDS |
| 98 | <i>Reserved</i> | LVDS |
| 100 | GPIO_PWM | VIO |
| 102 | Vcam_OUT | Vcam |
| 104 | SD_CMD | VIO |
| 106 | SD_D0 | VIO |
| 108 | SD_D2 | VIO |
| 110 | Vsysbus_OUT | Vsysbus |
| 112 | <i>Reserved</i> | Vsysbus |
| 114 | <i>Reserved</i> | Vsysbus |
| 116 | <i>Reserved</i> | Vsysbus |
| 118 | <i>Reserved</i> | Vsysbus |
| 120 | <i>Reserved</i> | Vsysbus |
| 122 | <i>Reserved</i> | Vsysbus |
| 124 | <i>Reserved</i> | Vsysbus |
| 126 | <i>Reserved</i> | Vsysbus |
| 128 | <i>Reserved</i> | Vsysbus |
| 130 | <i>Reserved</i> | Vsysbus |
| 132 | <i>Reserved</i> | Vsysbus |
| 134 | <i>Reserved</i> | Vsysbus |
| 136 | <i>Reserved</i> | Vsysbus |
| 138 | <i>Reserved</i> | Vsysbus |
| 140 | <i>Reserved</i> | Vsysbus |
| 142 | <i>Reserved</i> | Vsysbus |
| 144 | <i>Reserved</i> | Vsysbus |
| 146 | <i>Reserved</i> | Vsysbus |
| 148 | <i>Reserved</i> | Vsysbus |
| 150 | <i>Reserved</i> | Vsysbus |
| 152 | VIO_OUT | VIO |
| 154 | GPIO_A | VIO |
| 156 | GPIO_B | VIO |
| 158 | I2C2_CLK | VIO |
| 160 | I2C2_DATA | VIO |
| 162 | GPIO_C | VIO |
| 164 | GPIO_E | VIO |
| 166 | USB_OTG_VBUS | USB |
| 168 | USB_OTG_ID | USB |
| 170 | USB_OTG_D+ | USB |
| 172 | USB_OTG_D- | USB |
| 174 | USB_PWR_STAT | VIO |
| 176 | USB_PWR_EN | VIO |
| 178 | USB_HOST_D1+ | USB |
| 180 | USB_HOST_D1- | USB |
| 182 | I2C1_CLK | VIO |

| Pin number | Pin name | Power domain | Pin number | Pin name | Power domain |
|------------|-----------------|--------------|------------|------------------|--------------|
| 183 | SPI1_MOSI | VIO | 184 | I2C1_DATA | VIO |
| 185 | GND9 | Vin | 186 | nETH1_LINK_LED | VIO |
| 187 | nETH2_LINK_LED | VIO | 188 | nETH1_SPEED_LED | VIO |
| 189 | nETH2_SPEED_LED | VIO | 190 | ETH1_TXD- | Ethernet |
| 191 | ETH2_TXI- | Ethernet | 192 | ETH1_TXD+ | Ethernet |
| 193 | ETH2_TXI+ | Ethernet | 194 | ETH_VIO_SWITCHED | VIO |
| 195 | ETH2_RXI- | Ethernet | 196 | ETH1_RXI- | Ethernet |
| 197 | ETH2_RXI+ | Ethernet | 198 | ETH1_RXI+ | Ethernet |
| 199 | GND10 | Vin | 200 | VCC_BAT | Vbat |

Table 26: SODIMM-200 pin assignment

4.2 JTAG

4.2.1 FFC connector

| Pin number | Pin name |
|------------|-----------------|
| 1 | +3V3 Output |
| 2 | GND |
| 3 | JTAG_TMS |
| 4 | #JTAG_TRST |
| 5 | JTAG_TCK |
| 6 | JTAG_TDO |
| 7 | JTAG_TDI |
| 8 | #RESET_IN |
| 9 | <i>Reserved</i> |
| 10 | <i>Reserved</i> |

Table 27: FFC JTAG interface pin assignment

4.2.2 Tag-Connect

| Pin number | Pin name |
|------------|-----------------|
| 1 | +3V3 Output |
| 2 | JTAG_TMS |
| 3 | GND |
| 4 | JTAG_TCK |
| 5 | <i>Reserved</i> |
| 6 | JTAG_TDO |
| 7 | #JTAG_TRST |
| 8 | JTAG_TDI |
| 9 | <i>Reserved</i> |
| 10 | #RESET_IN |

Table 28: Tag-Connect JTAG interface pin assignment

5 Technical specifications

5.1 Operating conditions – Absolute maximum ratings

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------------|---|-----|-----|------|------|
| VCC (Vin) | Power supply voltage INPUT | 3.2 | | 5.5 | V |
| VCC _{ripple} (Vin) | VCC ripple peak-to-peak | | 50 | 100 | mV |
| V _{bat} | Battery voltage INPUT | 1.3 | | 4.0 | V |
| V _{sysbus} | System bus voltage OUTPUT | | 3.3 | | V |
| I _{sysbus} | V _{sysbus} current | | | 20 | mA |
| V _{disp} | Display voltage OUTPUT | | 3.3 | | V |
| I _{vdisp} | V _{disp} current | | | 20 | mA |
| V _{cam} | Camera voltage OUTPUT | | 3.3 | | V |
| I _{vcam} | V _{cam} current | | | 20 | mA |
| V _{io} | I/O voltage OUTPUT | | 3.3 | | V |
| I _{vio} | V _{io} current | | | 20 | mA |
| V _{ETH_VIO_SWITCHED} | ETH_VIO_SWITCHED voltage OUTPUT | | 3.3 | | V |
| I _{ETH_VIO_SWITCHED} | ETH_VIO_SWITCHED current | | | 60 | mA |
| I _{operating} | Operating current (without V*_OUT pins, VCC = 3.3V) | | 150 | tbd | mA |
| P _{operating} (Power) | Core module power consumption | | 0,5 | tbd | W |
| I _{Vbat} | V _{bat} input current | | | 5 | mA |
| I _{Vbat_Stby} | V _{bat} Standby input current | | 800 | 1000 | nA |
| V _{IH_3V3} | Digital input high voltage | 2.0 | 3.3 | | V |
| V _{IL_3V3} | Digital input low voltage | | 0 | 0.8 | V |

Table 29: DC operating conditions

5.2 Reset Timings

| Symbol | Description | Min | Typ | Max | Unit |
|-----------|---|-----|-----|-----|------|
| RESET_IN | System Reset input assertion time (active low) | 10 | | | ms |
| RESET_OUT | System Reset output assertion time (active low) | 10 | | | ms |

Table 30: Reset Timings

5.3 Dimensions

Notes:

- Figure 7 shows an example with 5,2mm SODIMM-200 socket height.

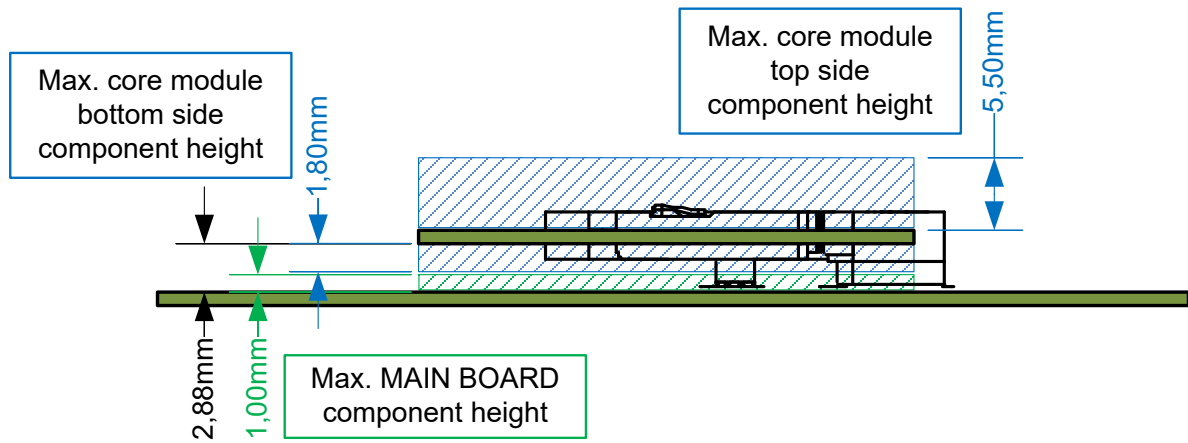


Figure 7: Maximum component heights

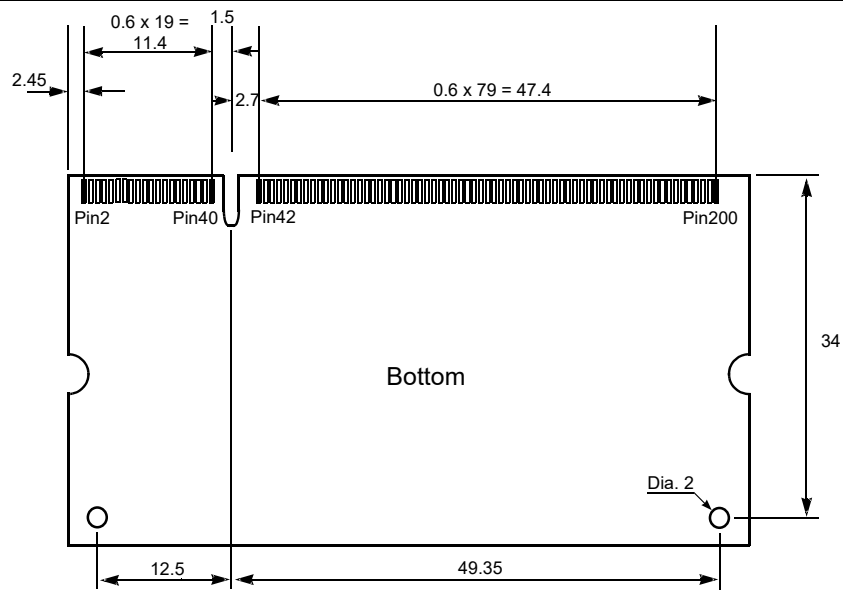
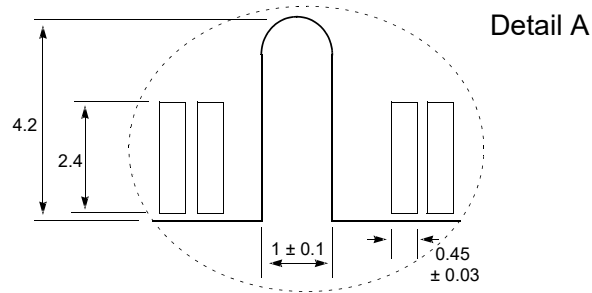
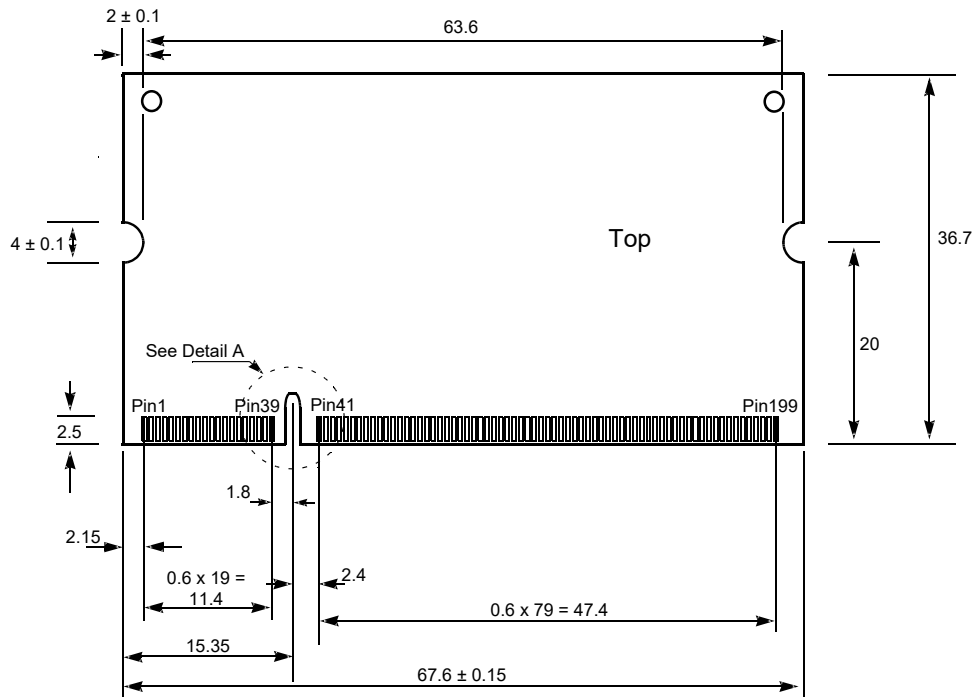


Figure 8: Dimensions of the module

5.4 Mechanical system

Several suggestions are given for the plugs, sockets and cables in the following subsections.

5.4.1 SODIMM-200 socket

The DHCM-iMX6UL(L)-01D2 module is designed for operation in a standard 2.5V (DDR) SODIMM-200 memory socket.

The following sockets have been successfully tested with the module:

| Manufacturer | Description | Article number |
|--|--|-----------------|
| Nexus Components http://www.nexus-de.com/ | <ul style="list-style-type: none"> Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm | 5214HB52 |
| E-tec Interconnect http://www.e-tec.ch/v3/ | <ul style="list-style-type: none"> Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm | DMD-200-RSE9-55 |
| Tyco Electronics http://www.tycoelectronics.com | <ul style="list-style-type: none"> Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm | 1473005-1 |
| Nexus Components http://www.nexus-de.com/ | <ul style="list-style-type: none"> Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm | 5214HB52 |
| E-tec Interconnect http://www.e-tec.ch/v3/ | <ul style="list-style-type: none"> Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm | DMD-200-RPE9-55 |
| Tyco Electronics http://www.tycoelectronics.com | <ul style="list-style-type: none"> Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm | 1612618-1 |

Table 31: SODIMM-200 sockets

5.4.2 JTAG FFC cable

| Manufacturer | Description | Article number |
|--|---|-----------------|
| Würth Elektronik http://www.we-online.com | <ul style="list-style-type: none"> 0.50 mm flat flexible cable Type 1 WR-FPC | 687 610 050 002 |
| Molex http://www.molex.com/ | <ul style="list-style-type: none"> 0.50mm flat flexible cable Type A | 982660097 |

Table 32: FFC Cable

5.5 Temperature range

| Symbol | Description | Min | Typ | Max | Unit |
|--------|--|-----|-----|-----|------|
| T_AMB | Operating temperature range | -40 | | 85 | °C |
| T_AMB | Operating temperature range with Murata 1DX (WiFi/BT) | -30 | | 70 | °C |

Table 33: Temperature range

6 RoHS conformance

This device has been manufactured RoHS II-compliant.