DHCOM AM335X

User Manual

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THE ART OF INNOVATION

Changes

Version	Date	Changes	Name
R01	2015-09-30	First version	SG
R02	2015-11-20	Added review	SG

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Abbreviations

- AIN = Analog input
- AINOUT = Analog input/output
- I = Input
- IO = Input/output
- MBC = Must be connected
- O = Output
- PD = Pull-Down
- PU = Pull-Up
- PWR_I = Power input
- PWR_O = Power output
- TBD = To be defined

1 Introduction

1.1 Hardware

The DHCM-AM335x module is a computer module in the SODIMM-200 form factor on the basis of a Cortex-A8 processor from Texas Instruments. The CPU is clocked up to 1 GHz and is equipped with up to 512 MByte DDR3-Memory and 16 GByte eMMC flash. Numerous interfaces are also available for communicating with the outside world, which are required in embedded systems.

The pin assignment of the SODIMM 200 socket and the Molex high speed connector is subject to the DHCOM standard, so that a replacement or an upgrade to other DHCOM modules is very easy possible.

1.2 Software

At present, following operating systems for the DHCM-AM335x module are available:

- Embedded Linux
- Android on request
- Windows Embedded Compact on request

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.

1.3 Main characteristics

- Texas Instruments ARM Cortex-A8 up to 1GHz
- 3D graphics accelerator
- 0 - 1024 MByte NAND flash memory (8 bit bus width) or 2 - 16 GByte eMMC flash
- 2Mbyte SPI flash
- 128 - 512 MByte DDR3 DRAM
- On-board microSD card socket
- SD/MMC card interface, 4 bit SDIO
- LC display controller, 24 bit colors, 2048 x 2048 pixels
- On-board touch controller for 4-wire resistive touch screens
- 2 x Ethernet controller 10/100 Mbit, IEEE1588 conform
- RGMII interface for Gbit Ethernet
- USB 2.0 OTG high-speed

- USB 2.0 host high speed
- 2 x Standard UART (1 x with hardware handshake support)
- CAN interface
- 2 x SPI interface
- I2C™ interface
- I²S Audio interface
- Real-time clock (I2C™ connection), low power temperature compensated
- 12 bit analog input
- 2 x 1 kbit EEPROM with integrated MAC address
- PWM channel
- 18 GPIOs
- JTAG debug connection via FFC plug connector
- Industrial temperature range (-40°C to +85°C)
- SODIMM-200 socket with DHCOM pin assignment
- Molex high speed socket with DHCOM-X pin assignment

1.4 CPU differences

Description	AM3352	AM3354	AM3358	AM3359
Package	15x15 /0.8mm	15x15 /0.8mm	15x15 /0.8mm	15x15 /0.8mm
CPU speed	Up to 1GHz	Up to 1GHz	Up to 1GHz	Up to 800MHz
Graphics Acceleration	-	3D Graphics	3D Graphics	3D Graphics
DMIPS	2000	2000	2000	1600
On-Chip L1 cache	64KB	64KB	64KB	64KB
On-Chip L2 cache	256KB	256KB	256KB	256KB
On-chip memory	128KB	128KB	128KB	128KB
PRU-ICSS	-	-	Dual Core PRU + standard protocols	Dual Core PRU + all protocols
Analog-to-digital converter	12-Bit	12-Bit	12-Bit	12-Bit

Table 1: CPU differences

1.5 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

1.5.1 Texas Instruments Cortex-A8 processor

Data sheets and technical documents can be found at http://www.ti.com/

1.5.2 Microchip ethernet PHY LAN8710Ai

Data sheets and technical documents can be found at https://www.microchip.com/

1.5.3 Micro Crystal real-time clock RV-3029-C3

Data sheets and technical documents can be found at http://www.microcrystal.com/

2 Hardware overview

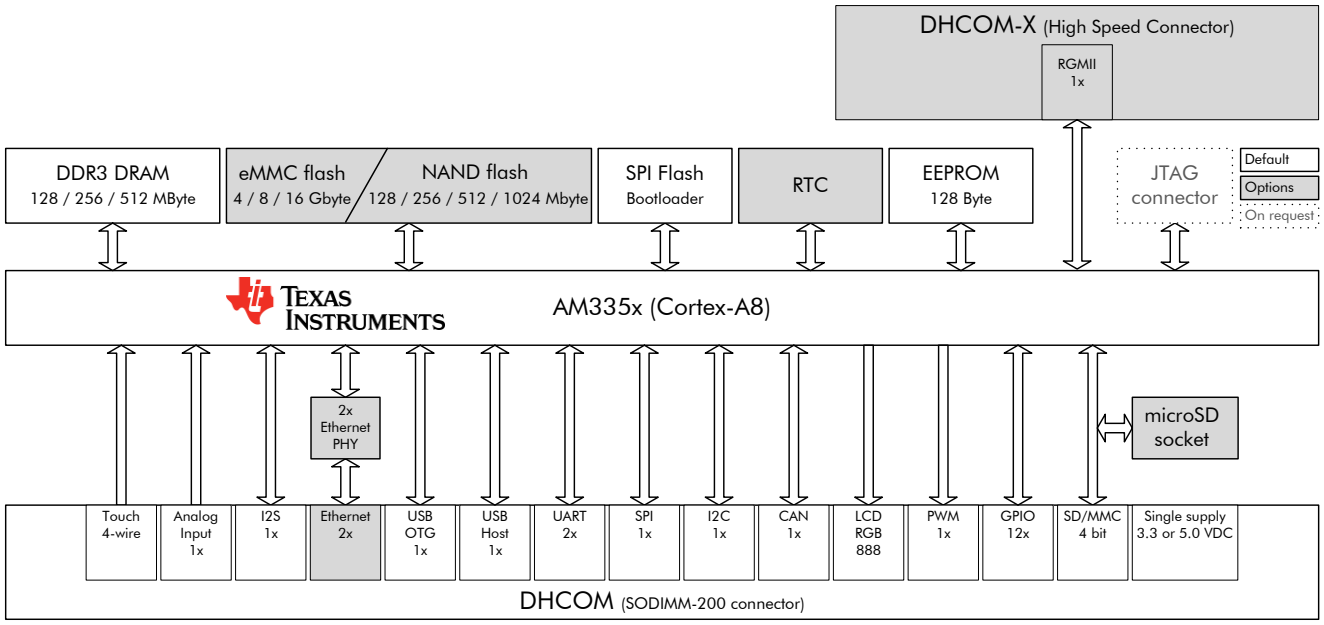

Figure 1: DHCM-AM335x block diagram

Figure 1 provides an overview of the DHCM-AM335x module. All interfaces and memory components are shown. All grayed blocks could be mounted optional on a specific customer core module.

3 Signal description

The following subsections describe the signals at the SODIMM-200 and Molex high speed socket. The **green** marked table columns belong to **DHCOM SODIMM-200** connector and the **red** marked to **DHCOM-X Molex high speed** connector.

Notes:

- For all specified pull-up and pull-down resistors, a value of 10k is recommended.
- "Not used" specification describes, what needs to be done with unconnected pins.

DHCOM hardware compatibility:

The DHCOM specification specifies function groups in order to ensure compatibility between various DHCOM modules. Each function group has its own voltage level output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters on the customer specific main board provide compatibility between various DHCOM modules. Naturally, these level shifters can also be removed from the customer design. In this case, the customer will lose compatibility to the DHCOM standard.

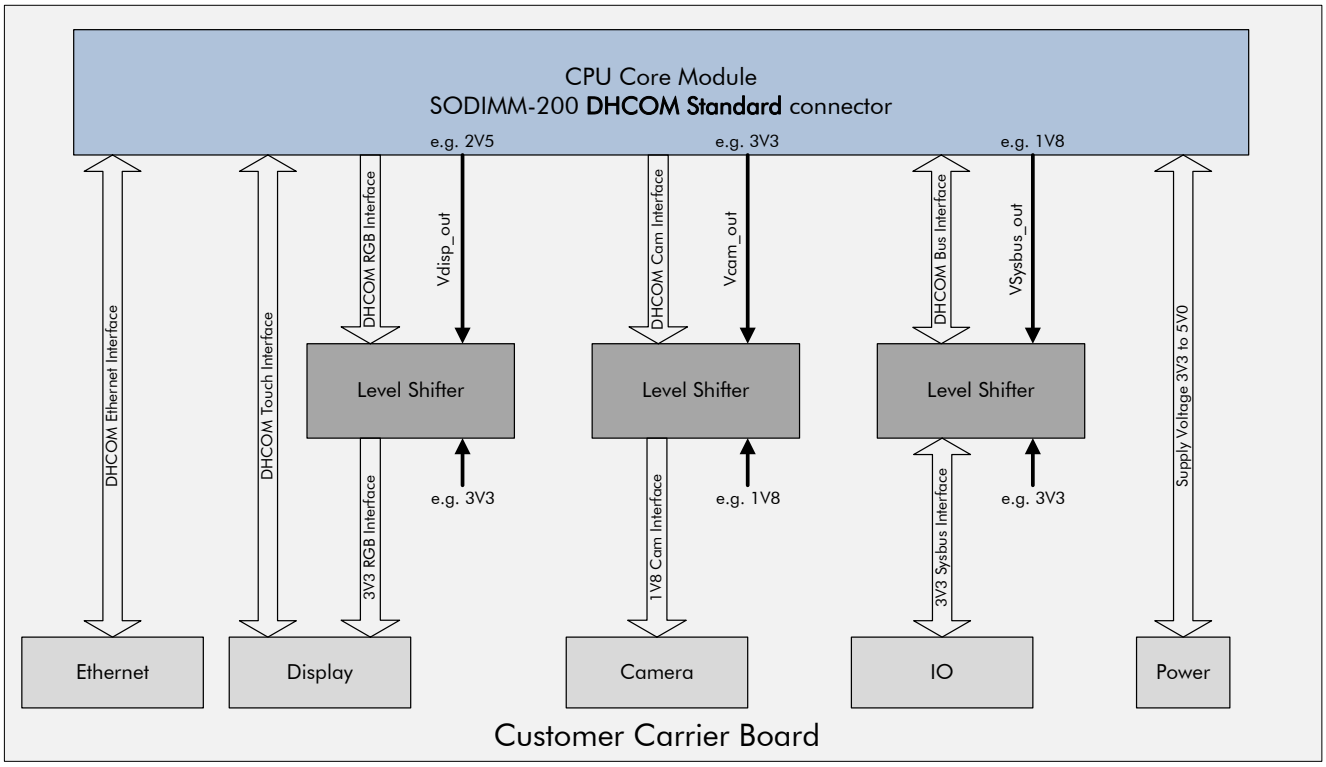

Figure 2: DHCOM functions groups concept

Important:

With the level shifter concept it is possible to support all core modules which are developed from DH electronics in the future. If you only like to use the current DHCOM modules (DHCOM i.MX25, AM35x, AM335x and i.MX6) you only need to use level shifters in special cases. Have a look at the following table:

Voltage	i.MX25	AM3517	AM335x	i.MX6
VCC (Vin)	3.2V – 5.5V	3.2V – 5.5V	3.2V – 5.5V	3.2V – 5.5V
Vbat	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V
Vsysbus	1.8V	3.3V	-	3.3V
Vdisp	3.3V	3.3V	3.3V	3.3V
Vcam	3.3V	3.3V	3.3V	3.3V
VIO	3.3V	3.3V	3.3V	3.3V
VETH_VIO_SWITCHED	3.3V	3.3V	3.3V	3.3V

Table 2: Voltage groups

Summary:

At the moment you only need level shifters at address and data bus interface, if you like to use parallel address and data bus, i.MX25 and another DHCOM core module in the same mainboard hardware.

3.1 Power supply and reset

3.1.1 Power supply

The DHCM-AM335x has the following power connections:

- Vin = Core module supply voltage input
- Vbat = Battery voltage input
- Vsysbus = System bus voltage output
- Vdisp = Display voltage output
- Vcam = Camera voltage output
- VIO = I/O voltage output
- VCC_RGMII_OUT = Supply voltage for Gbit PHY IO voltage

Note: When no buffer battery is used in the system, Vbat must be connected to 3.3V.

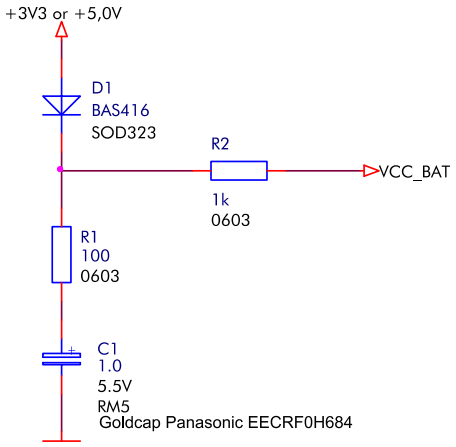

Figure 3: Vbat GoldCap example

The power supply connections Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT are to be used to detect the right voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with a level shifter.

3.1.2 Reset

The system is put in reset state by holding RESET_IN signal low.

When the RESET_IN is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_OUT are asserted as long as RESET_IN is asserted. If the reset input RESET_IN is de-asserted, the RESET_OUT is also de-asserted and the module starts booting again.

It is not necessary to held RESET_IN low during power-up.

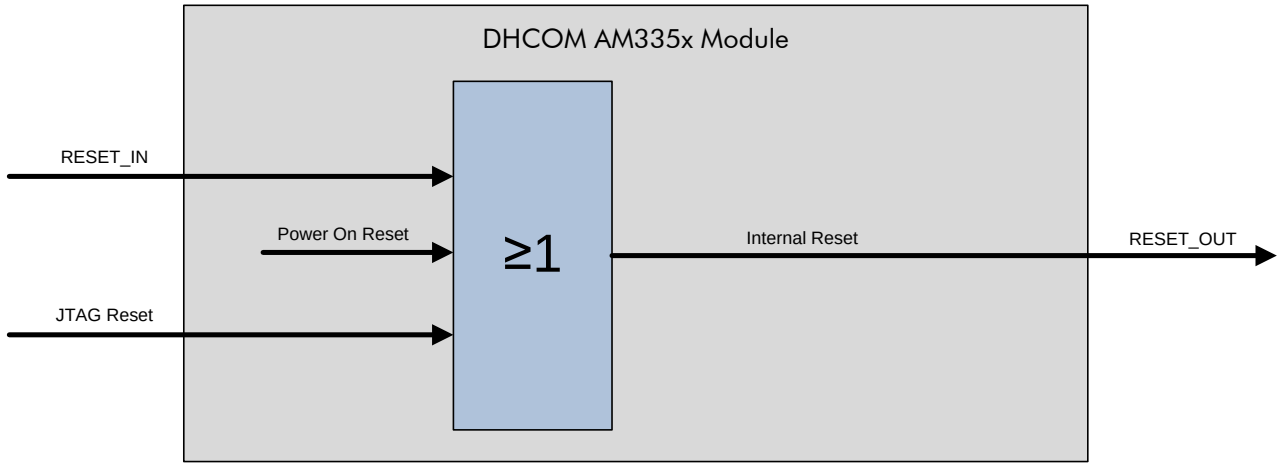

Figure 4: Reset

3.1.3 Signal Overview

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
VCC_IN1	Core Module supply voltage input	38	PWR_I	-	MBC
VCC_IN2	Core Module supply voltage input	39	PWR_I	-	MBC
VCC_IN3	Core Module supply voltage input	40	PWR_I	-	MBC
VCC_IN4	Core Module supply voltage input	41	PWR_I	-	MBC
VCC_IN5	Core Module supply voltage input	42	PWR_I	-	MBC
VCC_IN6	Core Module supply voltage input	44	PWR_I	-	MBC
GND1	Core Module Ground	17	PWR_I	-	MBC
GND2	Core Module Ground	19	PWR_I	-	MBC
GND3	Core Module Ground	43	PWR_I	-	MBC
GND4	Core Module Ground	45	PWR_I	-	MBC
GND5	Core Module Ground	47	PWR_I	-	MBC
GND6	Core Module Ground	101	PWR_I	-	MBC
GND7	Core Module Ground	111	PWR_I	-	MBC
GND8	Core Module Ground	153	PWR_I	-	MBC
GND9	Core Module Ground	185	PWR_I	-	MBC
GND10	Core Module Ground	199	PWR_I	-	MBC
VCC_BAT	Core Module Battery voltage input	200	PWR_I	-	MBC
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	-	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	-	MBC
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
Vcam_OUT	Camera supply voltage output	102	PWR_O	-	-
VIO_OUT	I/O supply voltage output	152	PWR_O	-	-
RESET_IN	System Reset input (active low)	21	I	-	-
RESET_OUT	System Reset output (active low)	20	O	-	-

Table 3: SODIMM-200 Power supply and reset

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball number	Not used
VCC_IN7	Core Module supply voltage input	79	PWR_I	-	MBC
VCC_IN8	Core Module supply voltage input	80	PWR_I	-	MBC
GND11	Core Module Ground	19	PWR_I		MBC
GND12	Core Module Ground	22	PWR_I		MBC
GND13	Core Module Ground	25	PWR_I		MBC
GND14	Core Module Ground	28	PWR_I		MBC
GND15	Core Module Ground	35	PWR_I	-	MBC
GND16	Core Module Ground	36	PWR_I	-	MBC
GND17	Core Module Ground	41	PWR_I	-	MBC
GND18	Core Module Ground	46	PWR_I	-	MBC
GND19	Core Module Ground	53	PWR_I	-	MBC
GND20	Core Module Ground	58	PWR_I	-	MBC
GND21	Core Module Ground	67	PWR_I	-	MBC
GND22	Core Module Ground	68	PWR_I	-	MBC
VCC_RGMII_OUT	3,3V Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	-	-

Table 4: DHCOM-X Power supply

3.2 Hardware coding

The following pins can be used to read out the current hardware version of the DHCOM AM335x core module.

CPU ball name	Description	CPU ball number	IO Type
GPMC_AD13	Code_HW_0	R12	I/O
GPMC_AD12	Code_HW_1	T12	I/O
GPMC_AD11	Code_HW_2	U12	I/O

Table 5: Hardware coding

DH PCB Numbers	Description	Code_HW_2	Code_HW_1	Code_HW_0
515-100	DHCOM AM335x without second Ethernet interface	0 (100k PD)	0 (100k PD)	0 (100k PD)
515-200 (current version)	DHCOM AM335x with second Ethernet interface	0 (100k PD)	0 (100k PD)	1 (100k PU)
515-300		0 (100k PD)	1 (100k PUD)	0 (100k PD)
515-400		0 (100k PD)	1 (100k PD)	1 (100k PU)
...		...	...	...

Table 6: Different hardware versions

3.3 Touch controller / Analog inputs

The DHCM-AM335x touch screen controller and analog-to-digital converter provides a low-cost resistive touch screen solution. The SODIMM module can be connected directly to a 4-wire touch panel. The AM335x also offers up to four auxiliary ADC inputs for analogue measurements such as temperature and light or monitor the battery voltage in portable systems. For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments. http://www.ti.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
TSPX	Resistive Touch: 4 wire (X +)	12	AINOUT	-	PD
TSMX	Resistive Touch: 4 wire (X -)	14	AINOUT	-	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	AINOUT	-	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	AINOUT	-	PD

Table 7: Touch controller connections

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
Analog_In0	Analog input 0	8	AIN	-	PD
Analog_In1	Analog input 1	6	AIN	-	PD
Analog_In2	Analog input 2	4	AIN	-	PD
Analog_In3	Analog input 3	2	AIN	-	PD

Table 8: Analog inputs

3.4 Ethernet

The AM335x processor includes two 10/100/1000 Ethernet Media Access Controller (MAC). Two 10/100 Ethernet transceiver (Microchip LAN8710Ai) are connected on the module. These Ethernet interfaces fulfil the IEEE 802.3 standard.

Instead of the second 10/100 Ethernet transceiver it is possible to connect the RGMII interface to the DHCOM-X Molex high speed connector. It is possible to connect these RGMII signals on a baseboard to a 10/100/1000 Ethernet transceiver (e.g. Micrel KSZ9021RN).

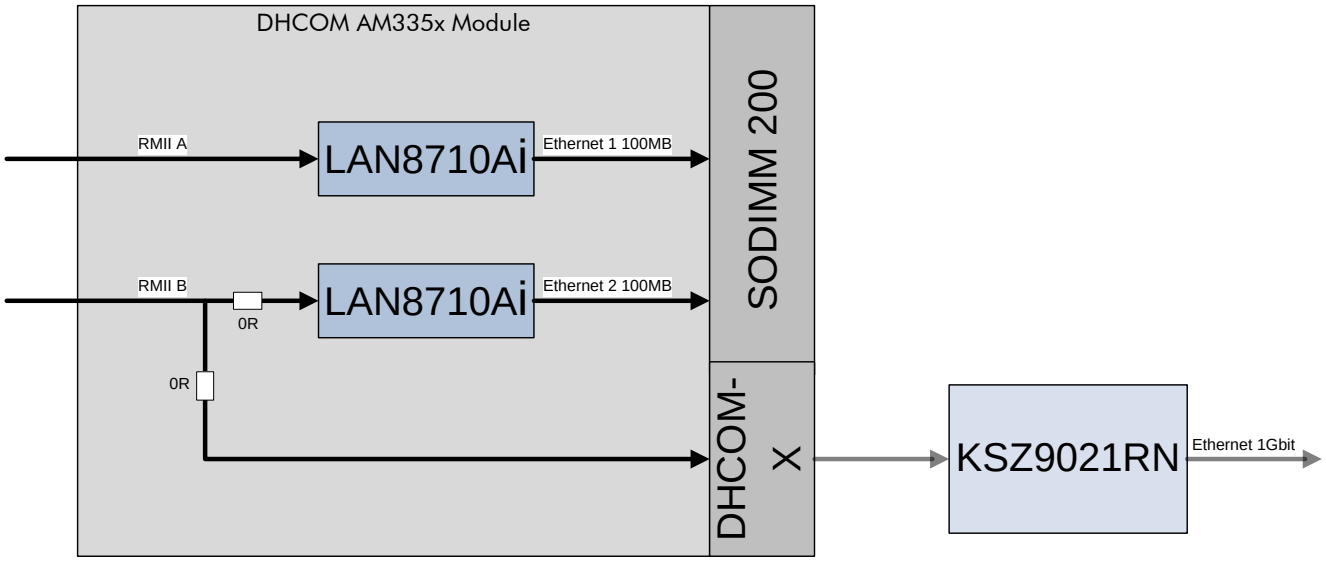

Figure 5: Ethernet

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments, Microchip and Micrel.

http://www.ti.com/

https://www.microchip.com/

http://www.micrel.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	-	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	-	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	-	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	-	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	-	-
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	-	PD

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	-	PD
nETH2_LINK_LED	Port 2: Activity LED connection	187	O	-	PD
nETH2_SPEED_LED	Port 2: Speed LED connection	189	O	-	PU
ETH2_TXD-	Port 2: Ethernet TX Differential Output (minus)	191	O	-	PD
ETH2_TXD+	Port 2: Ethernet TX Differential Output (plus)	193	O	-	PD
ETH2_RXI-	Port 2: Ethernet TX Differential Input (minus)	195	I	-	PD
ETH2_RXI+	Port 2: Ethernet TX Differential Input (plus)	197	I	-	PD

Table 9: 100Mbit Ethernet connections

Note: The LED outputs "nETH1_LINK_LED", "nETH1_SPEED_LED" and "nETH2_LINK_LED", "nETH2_SPEED_LED" must be connected as follows:

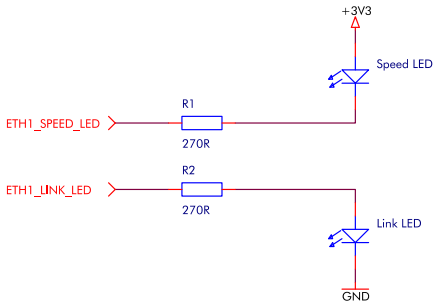

Figure 6: Ethernet LEDs

Note: In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration lines.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball number	Not used
RGMII_RXCLK	RGMII receive clock, 125 MHz digital	1	I	T15	
RGMII_RXD0	RGMII received data 0	3	I	V17	
RGMII_RXD1	RGMII received data 1	5	I	T16	
RGMII_RXD2	RGMII received data 2	7	I	U16	
RGMII_RXD3	RGMII received data 3	9	I	V16	
RGMII_RX_CTL	RGMII receive data valid	11	I	V14	
RGMII_MDIO	Management data	13	IO	M17	
RGMII_RST	*Not connected, just PU*	15	O		
RGMII_WOL_INT	*Not connected*	17	I		PU
RGMII_TXCLK	RGMII transmit clock, 125 MHz digital	2	O	U15	
RGMII_TXD0	RGMII transmit data 0	4	O	V15	
RGMII_TXD1	RGMII transmit data 1	6	O	R14	
RGMII_TXD2	RGMII transmit data 2	8	O	T14	
RGMII_TXD3	RGMII transmit data 3	10	O	U14	
RGMII_TX_CTL	RGMII transmit enable	12	O	R13	

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball number	Not used
RGMII_MDC	Management data clock	14	O	M18	
RGMII_REFCLK	*Not connected, just PD*	16	O		
RGMII_INT	PHY interrupt (active low)	18	I	C14	PU
VCC_RGMII_OUT	Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O		

Table 10: RGMII Interface

3.5 USB

The DHCM-AM335x module supports a maximum of two USB devices. These consist of a USB OTG connection and a USB host connection. For both connections the integrated AM335x PHYs are used.

All two ports are high-speed USB connections, which also support full speed and low speed.

3.5.1 USB OTG

This USB interface fulfils the USB 2.0 specification. It can be configured as OTG, host or device. As a host, it supports peripheral devices of all speeds and as a peripheral, it communicates at either high-speed (480Mbps) or full speed (12Mbps) when connected to legacy host computers.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
USB_OTG_VBUS	OTG Client: VBUS Input line OTG Host: USB bus supply voltage	166	I / PWR_O	P15	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	P16	-
USB_OTG_D+	USB OTG differential Signal positive line	170	IO	N17	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	IO	N18	PD

Table 10: USB OTG

Note: The DHCOM USB OTG port does not provide any "enable" and "over current" signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event, the "over current" output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

3.5.2 USB Host

The USB Host port fulfils the USB 2.0 specification. It supports high-speed, full speed and low speed data transfers.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
USB_PWR_STAT	USB Host over current indicator (active low)	174	I	J17	-
USB_PWR_EN	USB Host power enable signal (active low)	176	O	F15	-
USB_HOST_D1+	USB Host differential Signal positive line	178	IO	R17	PD

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
USB_HOST_D1-	USB Host differential Signal negative line	180	IO	R18	PD

Table 11: USB Host

3.6 UART

The DHCM-AM335x module offers in total two UART connections. UART 1 with additionally hardware handshake and UART 2.

The maximum transfer rate is 3.68 Mbaud/s.

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

http://www.ti.com/

3.6.1 UART 1

Note: DHCOM UART 1 is the UART 0 module of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
UART1_CTS	UART clear to send	24	I	E18	-
UART1_RTS	UART request to send	26	O	E17	-
UART1_RX	UART receive data line	32	I	E15	-
UART1_TX	UART transmit data line	34	O	E16	-

Table 12: UART 1

Hardware design notes: It is essential to create always a connection to DHCOM UART 1, since the DHCOM bootloader can be configured with the UART 1. A minimum connection possibility should be made available via solder pads.

3.6.2 UART 2

Note: DHCOM UART 2 is the UART 1 module of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
UART2_RX	UART receive data line	35	I	D16	-
UART2_TX	UART transmit data line	37	O	D15	-

Table 13: UART 2

3.7 Serial port interface

The DHCM-AM335x module is equipped with two SPI interfaces. These interfaces consist of a full duplex capable, 4-wire interface and have the following characteristics:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to 48MHz

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

http://www.ti.com/

3.7.1 SPI 1

Notes:

- DHCOM SPI Port 1 is connected to the SPI0 interface of the AM335x
- SPI1_CS0 on the SODIMM-200 socket uses the SPI0_CS1 signal of the AM335x
- The SPI0 interface of the AM335x is also used for the on-board SPI flash
- SPI0_CS0 is used for the on-board SPI flash

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
SPI1_CS0	Slave select signal	177	O	C15	-
SPI1_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	A17	-
SPI1_MISO	SSP receive data line	181	I	B17	-
SPI1_MOSI	SSP transmit data line	183	O	B16	-

Table 14: SPI1 Interface

3.7.2 SPI 2

There is the possibility to use some GPIOs (GPIO_F, GPIO_G, GPIO_H, GPIO_I) instead of general purpose input-output signals as an additional serial peripheral interface. There is a special component variant for this functionality. The standard component variant uses the GPIO functionality.

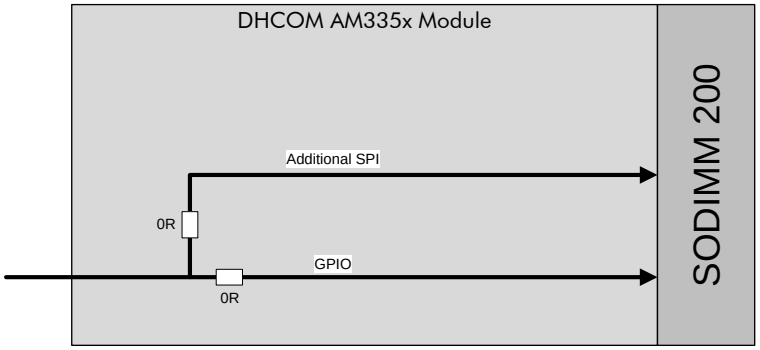

Figure 7: SPI2 variant

Notes:

- DHCOM SPI Port 2 is connected to the SPI1 interface of the AM335x
- SPI2_CS0 on the SODIMM-200 socket uses the SPI1_CS0 signal of the AM335x

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
SPI2_CS0	Slave select signal	155	O	C12	-
SPI2_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	157	IO	C18	-
SPI2_MISO	SSP receive data line	159	I	B13	-
SPI2_MOSI	SSP transmit data line	161	O	D12	-

Table 15: SPI2 Interface

3.8 I²C™

The DHCM-AM335x module provides the opportunity to connect an I2CTM multimaster bus. The I2CTM bus controller integrated in the AM335x has the following main features:

- Compatibility with I2C bus standard
- Multiple-master operation
- Supports standard mode (up to 100Kbits/s) and fast mode (up to 400Kbits/s)
- Programmable clock generation
- 7-Bit and 10-Bit device addressing modes
- Built-in 32-byte FIFO for buffered read or writes

The pull-up resistors required according to the I2CTM specification are already fitted on the module. For detailed information about I2CTM, reference is made to the specification (Philips Semiconductor):

http://www.nxp.com

3.8.1 I2C1

Note: DHCOM I2C1 uses the I2C2 instance of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
I2C1_CLK	I²C clock line	182	IO	D17	-
I2C1_DATA	I²C data line	184	IO	D18	-

Table 16: I2C1 Interface

3.8.2 I2C0

Note: The I2C0 instance (I2C0_SCL = CPU ball "C16", I2C0_SDA = CPU ball "C17") of the AM335x is used on the core module for following components:

- RTC EEPROM (7bit address: 0x56)
- MAC EEPROM1 (7bit address: 0x53)
- MAC EEPROM2 (7bit address: 0x50)
- PMIC (7bit address: 0x12)

3.9 CAN

The AM335x processor has an integrated standard resp. high-end CAN controller with the following characteristics:

- Supports CAN protocol version 2.0 A, B
- Programmable bit rate up to 1 Mbit/s
- 16, 32, 64 or 128 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend module reset
- Automatic bus on after Bus-Off state by programmable 32-bit timer
- CAN Rx / Tx pins configurable as general purpose IO pins
- DMA support

Note: DHCOM CAN uses the DCAN0 instance of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
CAN_TX	CAN transmit data line	27	O	J18	-
CAN_RX	CAN receive data line	29	I	K15	-

Table 17: CAN Interface

3.10 Audio Interface

The DHCM-AM335x module is equipped with one I2S interface for audio codec connection. This interface has the following characteristics:

- Support for I2S master mode
- Maximum audio sampling rate of 192kHz
- Compliant to Inter-IC Sound (I2S) bus specification from Philips

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

http://www.ti.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
I2S_RXD	Data receive signal	5	I	L16	PD
I2S_TXFS	Transmit Frame sync signal	11	O	L18	-
I2S_TXD	Data transmit signal	15	O	L17	-
I2S_TXC	Transmit clock signal	13	O	K18	-

Table 18: Audio interface

Note: If the audio inputs are not used, they must be closed with a pull-down. The resistor must be connected with VSSA_Audio.

3.11 Display

3.11.1 RGB

The DHCM-AM335x module enables the connection of a 24 bit LCD display. Active as well as passive LCD displays with a resolution of up to 2048 x 2048 pixels can be operated. A parallel RGB888 interface can be used to connect the core module to a display.

The core of the LCD controller is the integrated display subsystem in the AM335x. More precise information about this is available in the AM335x Reference Manual:

http://www.ti.com/

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
LC_R0	LCD display data red 0	76	O	T11	- (*)
LC_R1	LCD display data red 1	78	O	R12	- (*)
LC_R2	LCD display data red 2	49	O	U13	- (*)

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
LC_R3	LCD display data red 3	51	O	R1	- (*)
LC_R4	LCD display data red 4	53	O	R2	- (*)
LC_R5	LCD display data red 5	55	O	R3	- (*)
LC_R6	LCD display data red 6	57	O	R4	- (*)
LC_R7	LCD display data red 7	59	O	T1	- (*)
LC_G0	LCD display data green 0	80	O	T10	- (*)
LC_G1	LCD display data green 1	82	O	T12	- (*)
LC_G2	LCD display data green 2	61	O	T2	- (*)
LC_G3	LCD display data green 3	63	O	T3	- (*)
LC_G4	LCD display data green 4	65	O	T4	- (*)
LC_G5	LCD display data green 5	67	O	U1	- (*)
LC_G6	LCD display data green 6	69	O	U2	- (*)
LC_G7	LCD display data green 7	71	O	U3	- (*)
LC_B0	LCD display data blue 0	84	O	U10	- (*)
LC_B1	LCD display data blue 1	86	O	U12	- (*)
LC_B2	LCD display data blue 2	73	O	V13	- (*)
LC_B3	LCD display data blue 3	75	O	U4	- (*)
LC_B4	LCD display data blue 4	77	O	V2	- (*)
LC_B5	LCD display data blue 5	79	O	V3	- (*)
LC_B6	LCD display data blue 6	81	O	V4	- (*)
LC_B7	LCD display data blue 7	83	O	T5	- (*)
LC_EN	LCD display data enable	85	O	R6	- (*)
LC_VSYNC	LCD frame or vertical sync. puls	87	O	U5	- (*)
LC_HSYNC	LCD line or horizontal sync. puls	89	O	R5	- (*)
LC_PCLK	LCD pixel clock	91	O	V5	- (*)
GPIO_PWM	LCD contrast (only if PWM is not used)	100	O	A13	-

Table 19: RGB Interface

Note: (*) Regarding EMC it is recommended to terminate RGB interface lines with PD resistor.

3.12 PWM

The DHCM-AM335x module enables the connection to Pulse Width Modulation (PWM) output.

More precise information about this is available in the AM335x Reference Manual:

http://www.ti.com/

Note: DHCOM PWM uses the PWM1 instance of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
GPIO_PWM	PWM channel (only if LCD contrast is not used)	100	O	A13	-

Table 20: PWM Interface

3.13 SD/MMC/SDIO controller

The AM335x processor has a SD/MMC/SDIO card host controller integrated. The controller is used to connect a SD/MMC/SDIO interface to the SODIMM-200 socket.

There is a special component variant:

It is possible to buy the DHCOM module with assembled microSD socket. In this case the SD/MMC/SDIO card host controller is used to connect the module with the microSD socket and the SD/MMC/SDIO interface to the SODIMM-200 socket can't be used anymore.

It is just possible the use either the microSD socket or the interface to the SODIMM-200!

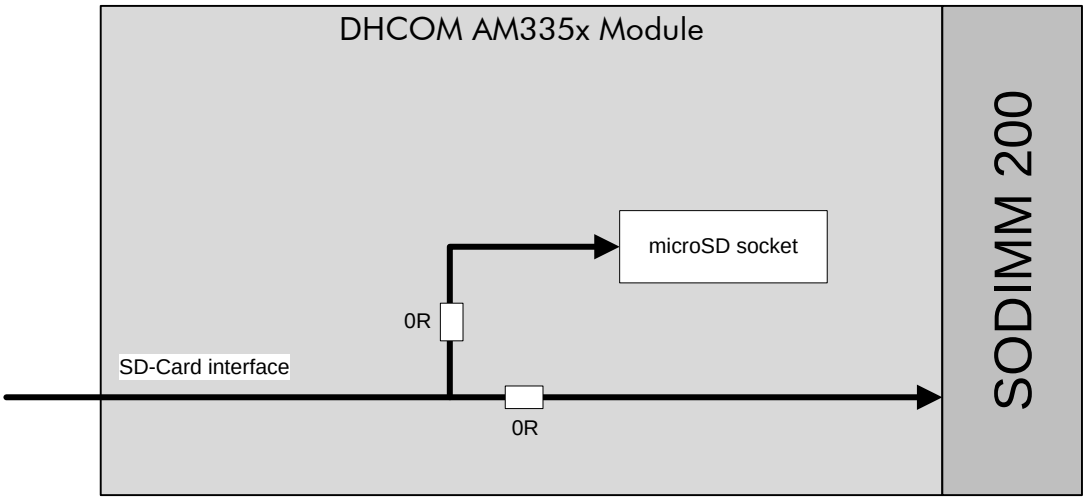

Figure 8: SD card interface

Main characteristics:

- Compatible with the MMC System specification version 4.3
- Conforms to the SD Physical Layer specification version 2.0
- Compatible with the SDIO Card Specification version 2.0
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit MMC modes
- Supports single block/multi-block read and write
- ...

3.13.1 SD/MMC/SDIO interface or On-board microSD socket

Note: DHCOM SD interface uses the MMC0 instance of the AM335x. The card detect pin uses a GPIO of the AM335x.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	G17	-
SD_CMD	SD/SDIO/MMC command line	104	IO	G18	-
SD_D0	SD/SDIO/MMC data line	106	IO	G16	-
SD_D1	SD/SDIO/MMC data line	107	IO	G15	-
SD_D2	SD/SDIO/MMC data line	108	IO	F18	-
SD_D3	SD/SDIO/MMC data line	109	IO	F17	-
SD_DETECT	GPIO_AM335x_8 (active high)	105	I	B14	PD

Table 21: SD/MMC/SDIO Interface

3.14 GPIOs

The DHCM-AM335x module provides several GPIO pins on the SODIMM-200 socket.

Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHCOM standard.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball number	Out of reset state	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low) GPIO0_19	151	IO	A15	In / PD	PU
GPIO _A	General Purpose I/O GPIO0_20	154	IO	D14	In / PD	-
GPIO _B	General Purpose I/O GPIO3_19	156	IO	C13	In / PD	-
GPIO _C	General Purpose I/O GPIO3_20	162	IO	D13	In / PD	-
GPIO _D	General Purpose I/O GPIO2_1	163	IO	V12	In / PD	-
GPIO _E	General Purpose I/O GPIO3_18	164	IO	B12	In / PD	-
GPIO _F	General Purpose I/O GPIO3_16	165	IO	D12	In / PD	-
GPIO _G	General Purpose I/O GPIO3_15	167	IO	B13	In / PD	-
GPIO _H	General Purpose I/O GPIO0_7	173	IO	C18	In / PD	-
GPIO _I	General Purpose I/O GPIO3_17	175	IO	C12	In / PD	-
VIO_OUT	Voltage for external Level-Shifter	152	PWR_O		-	-
GPIO_J	General Purpose I/O GPIO3_21	74	IO	A14	In / PD	-
GPIO_K	General Purpose I/O GPIO1_25	72	IO	U16	In / PD	-
GPIO_L	General Purpose I/O GPIO1_24	70	IO	V16	In / PD	-
GPIO_M	General Purpose I/O GPIO1_23	68	IO	T15	In / PD	-
GPIO_N	General Purpose I/O GPIO1_22	66	IO	U15	In / PD	-
GPIO_O	General Purpose I/O GPIO1_19	64	IO	T14	In / PD	-
GPIO_P	General Purpose I/O GPIO1_18	62	IO	U14	In / PD	-
GPIO_Q	General Purpose I/O GPIO1_17	60	IO	V14	In / PD	-
Vcam_OUT	Voltage for external Level-Shifter	102	PWR_O	-	-	-

Table 22: GPIO pin assignment

Note: There is the possibility to use some GPIOs instead of general purpose input-output signals as signals for other interfaces:

- If the RGMII interface on the DHCOM-X connector is used, the GPIOs K, L, M, N, O, P and Q are **NOT** available as GPIOs
- If the SPI2 interface on the SODIMM-200 connector is used, the GPIOs F, G, H and I are **NOT** available as GPIOs

There are special component variants for these functionalities. The standard component variant uses the GPIO functionality.

The GPIOs of the AM335x can only drive at a maximum of roughly 6mA (depends on the pad drive strength). Where a greater current is required, an additional driver must be provided on the carrier board. The minimum and maximum logic level can be obtained from the data sheet of the AM335x.

http://www.ti.com/

4 Plugs and connections

Additionally to the SODIMM-200 connector, the DHCM-AM335x module is equipped with Molex high speed connector, additional a 10pin FFC JTAG connector and a separate microSD card socket are available.

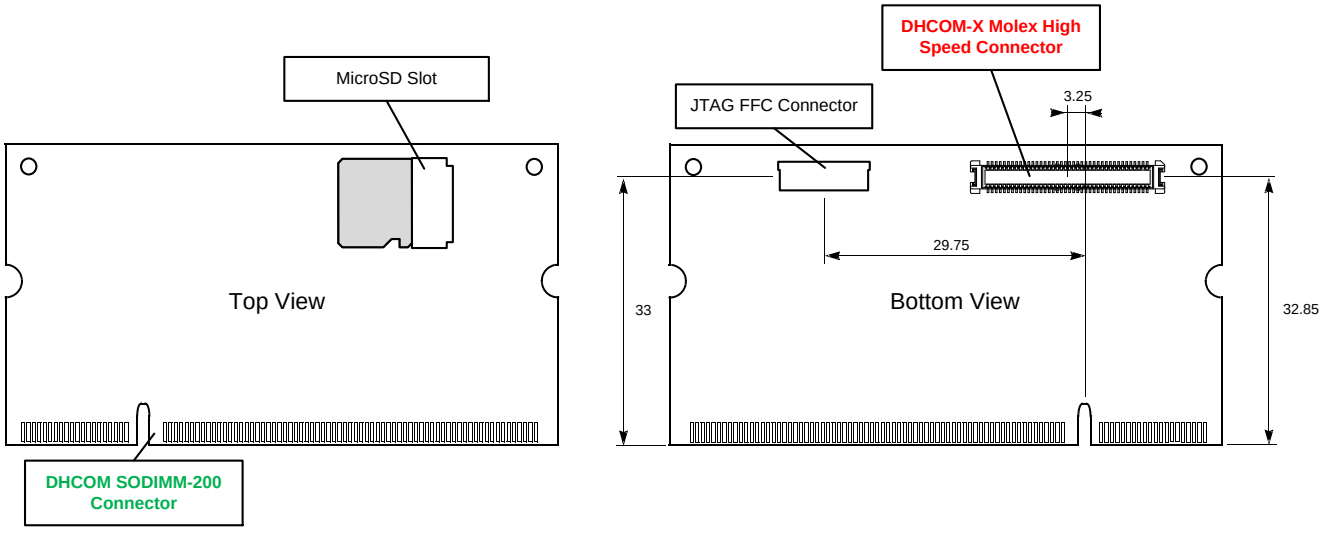

Figure 9: Position of plugs and connections

4.1 SODIMM-200

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
1	*Reserved*	VDDA	2	Analog Input 3	VDDA
3	*Reserved*	VDDA	4	Analog Input 2	VDDA
5	I2S_RXD	VIO	6	Analog Input 1	VDDA
7	*Reserved*	VDDA	8	Analog Input 0	VDDA
9	*Reserved*	VDDA	10	VDDA (Audio Supply VCC)	VDDA
11	I2S_TXFS	VIO	12	TSPX	VDDA
13	I2S_TXC	VIO	14	TSMX	VDDA
15	I2S_TXD	VIO	16	TSMY	VDDA
17	GND1	Vin	18	TSPY	VDDA
19	GND2	Vin	20	RESET_OUT	VIO
21	RESET_IN	VIO	22	*Reserved*	VIO
23	*Reserved*	VIO	24	UART1_CTS	VIO
25	*Reserved*	VIO	26	UART1_RTS	VIO
27	CAN_TX	VIO	28	*Reserved*	VIO
29	CAN_RX	VIO	30	*Reserved*	VIO
31	*Reserved*	VIO	32	UART1_RX	VIO
33	*Reserved*	VIO	34	UART1_TX	VIO
35	UART2_RX	VIO	36	*Reserved*	VIO
37	UART2_TX	VIO	38	VCC_IN1	Vin
39	VCC_IN2	Vin	40	VCC_IN3	Vin
41	VCC_IN4	Vin	42	VCC_IN5	Vin
43	GND3	Vin	44	VCC_IN6	Vin
45	GND4	Vin	46	Vdisp_OUT	Vdisp
47	GND5	Vin	48	*Reserved*	Vcam
49	LC_R2	Vdisp	50	*Reserved*	Vcam
51	LC_R3	Vdisp	52	*Reserved*	Vcam
53	LC_R4	Vdisp	54	*Reserved*	Vcam
55	LC_R5	Vdisp	56	*Reserved*	Vcam
57	LC_R6	Vdisp	58	*Reserved*	Vcam
59	LC_R7	Vdisp	60	GPIO_Q (or CIF_D6)	Vcam
61	LC_G2	Vdisp	62	GPIO_P (or CIF_D7)	Vcam
63	LC_G3	Vdisp	64	GPIO_O (or CIF_D8)	Vcam
65	LC_G4	Vdisp	66	GPIO_N (or CIF_D9)	Vcam
67	LC_G5	Vdisp	68	GPIO_M (or CIF_VSYNC)	Vcam
69	LC_G6	Vdisp	70	GPIO_L (or CIF_MCLK)	Vcam
71	LC_G7	Vdisp	72	GPIO_K (or CIF_PCLK)	Vcam
73	LC_B2	Vdisp	74	GPIO_J (or CIF_HSYNC)	Vcam
75	LC_B3	Vdisp	76	LC_R0	Vdisp
77	LC_B4	Vdisp	78	LC_R1	Vdisp
79	LC_B5	Vdisp	80	LC_G0	Vdisp
81	LC_B6	Vdisp	82	LC_G1	Vdisp
83	LC_B7	Vdisp	84	LC_B0	Vdisp
85	LC_EN	Vdisp	86	LC_B1	Vdisp
87	LC_VSYNC	Vdisp	88	*Reserved*	LVDS

Pin number	Pin name	Power domain
89	LC_HSYNC	Vdisp
91	LC_PCLK	Vdisp
93	*Reserved*	LVDS
95	*Reserved*	LVDS
97	*Reserved*	LVDS
99	*Reserved*	LVDS
101	GND6	Vin
103	SD_CLK	VIO
105	SD_DETECT	VIO
107	SD_D1	VIO
109	SD_D3	VIO
111	GND7	Vin
113	*Reserved*	Vsysbus
115	*Reserved*	Vsysbus
117	*Reserved*	Vsysbus
119	*Reserved*	Vsysbus
121	*Reserved*	Vsysbus
123	*Reserved*	Vsysbus
125	*Reserved*	Vsysbus
127	*Reserved*	Vsysbus
129	*Reserved*	Vsysbus
131	*Reserved*	Vsysbus
133	*Reserved*	Vsysbus
135	*Reserved*	Vsysbus
137	*Reserved*	Vsysbus
139	*Reserved*	Vsysbus
141	*Reserved*	Vsysbus
143	*Reserved*	Vsysbus
145	*Reserved*	Vsysbus
147	*Reserved*	Vsysbus
149	*Reserved*	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO
153	GND8	Vin
155	SPI2_CS0 (special component variant)	VIO
157	SPI2_CLK (special component variant)	VIO
159	SPI2_MISO (special component variant)	VIO
161	SPI2_MOSI (special component variant)	VIO
163	GPIO_D	VIO
165	GPIO_F	VIO
167	GPIO_G	VIO
169	*Reserved*	USB
171	*Reserved*	USB
173	GPIO_H	VIO
175	GPIO_I	VIO
177	SPI1_CS0	VIO
179	SPI1_CLK	VIO
181	SPI1_MISO	VIO

Pin number	Pin name	Power domain
90	*Reserved*	LVDS
92	*Reserved*	LVDS
94	*Reserved*	LVDS
96	*Reserved*	LVDS
98	*Reserved*	LVDS
100	GPIO_PWM	VIO
102	Vcam_OUT	Vcam
104	SD_CMD	VIO
106	SD_D0	VIO
108	SD_D2	VIO
110	*Reserved*	Vsysbus
112	*Reserved*	Vsysbus
114	*Reserved*	Vsysbus
116	*Reserved*	Vsysbus
118	*Reserved*	Vsysbus
120	*Reserved*	Vsysbus
122	*Reserved*	Vsysbus
124	*Reserved*	Vsysbus
126	*Reserved*	Vsysbus
128	*Reserved*	Vsysbus
130	*Reserved*	Vsysbus
132	*Reserved*	Vsysbus
134	*Reserved*	Vsysbus
136	*Reserved*	Vsysbus
138	*Reserved*	Vsysbus
140	*Reserved*	Vsysbus
142	*Reserved*	Vsysbus
144	*Reserved*	Vsysbus
146	*Reserved*	Vsysbus
148	*Reserved*	Vsysbus
150	*Reserved*	Vsysbus
152	VIO_OUT	VIO
154	GPIO_A	VIO
156	GPIO_B	VIO
158	*Reserved*	VIO
160	*Reserved*	VIO
162	GPIO_C	VIO
164	GPIO_E	VIO
166	USB_OTG_VBUS	USB
168	USB_OTG_ID	USB
170	USB_OTG_D+	USB
172	USB_OTG_D-	USB
174	USB_PWR_STAT	VIO
176	USB_PWR_EN	VIO
178	USB_HOST_D1+	USB
180	USB_HOST_D1-	USB
182	I2C1_CLK	VIO

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
183	SPI1_MOSI	VIO	184	I2C1_DATA	VIO
185	GND9	Vin	186	nETH1_LINK_LED	VIO
187	nETH2_LINK_LED	VIO	188	nETH1_SPEED_LED	VIO
189	nETH2_SPEED_LED	VIO	190	ETH1_TXD-	Ethernet
191	ETH2_TXD-	Ethernet	192	ETH1_TXD+	Ethernet
193	ETH2_TXD+	Ethernet	194	ETH_VIO_SWITCHED	VIO
195	ETH2_RXI-	Ethernet	196	ETH1_RXI-	Ethernet
197	ETH2_RXI+	Ethernet	198	ETH1_RXI+	Ethernet
199	GND10	Vin	200	VCC_BAT	Vbat

Table 23: SODIMM-200 pin assignment

4.2 DHCOM-X

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
1	RGMII_RXCLK	Vrgmii	2	RGMII_TXCLK	Vrgmii
3	RGMII_RXD0	Vrgmii	4	RGMII_TXD0	Vrgmii
5	RGMII_RXD1	Vrgmii	6	RGMII_TXD1	Vrgmii
7	RGMII_RXD2	Vrgmii	8	RGMII_TXD2	Vrgmii
9	RGMII_RXD3	Vrgmii	10	RGMII_TXD3	Vrgmii
11	RGMII_RX_CTL	Vrgmii	12	RGMII_TX_CTL	Vrgmii
13	RGMII_MDIO	Vrgmii	14	RGMII_MDC	Vrgmii
15	RGMII_RST (not connected, just a PD)	Vrgmii	16	RGMII_REFCLK (not connected, just a PD)	Vrgmii
17	*Reserved*	3V3	18	RGMII_INT	3V3
19	GND	Vin	20	VCC_RGMII_OUT	Vrgmii
21	*Reserved*	Sata	22	GND	Vin
23	*Reserved*	Sata	24	*Reserved*	Sata
25	GND	Vin	26	*Reserved*	Sata
27	*Reserved*	PCIe	28	GND	Vin
29	*Reserved*	PCIe	30	*Reserved*	PCIe
31	*Reserved*	PCIe	32	*Reserved*	PCIe
33	*Reserved*	PCIe	34	*Reserved*	3V3
35	GND	Vin	36	GND	Vin
37	*Reserved*	CSI	38	*Reserved*	CSI
39	*Reserved*	CSI	40	*Reserved*	CSI
41	GND	Vin	42	*Reserved*	CSI
43	*Reserved*	HDMI	44	*Reserved*	CSI
45	*Reserved*	HDMI	46	GND	Vin
47	*Reserved*	HDMI	48	*Reserved*	HDMI
49	*Reserved*	HDMI	50	*Reserved*	HDMI
51	*Reserved*	2V5	52	*Reserved*	HDMI
53	GND	Vin	54	*Reserved*	HDMI
55	*Reserved*	LVDS	56	*Reserved*	2V5
57	*Reserved*	LVDS	58	GND	Vin
59	*Reserved*	LVDS	60	*Reserved*	LVDS
61	*Reserved*	LVDS	62	*Reserved*	LVDS
63	*Reserved*	LVDS	64	*Reserved*	LVDS
65	*Reserved*	LVDS	66	*Reserved*	LVDS
67	GND	Vin	68	GND	Vin
69	*reserved*		70	*reserved*	
71	*reserved*		72	*reserved*	
73	*reserved*		74	*reserved*	
75	*reserved*		76	*reserved*	
77	*reserved*		78	*reserved*	
79	VCC_IN7	Vin	80	VCC_IN8	Vin

Table 24: DHCOM-X (Molex High Speed Connector)

4.3 JTAG

Pin number	Pin name
1	+3V3 Output
2	GND
3	JTAG_TMS
4	#JTAG_TRST
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	*Reserved*
10	*Reserved*

Table 25: JTAG interface pin assignment

5 Technical specifications

5.1 Operating conditions – Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT		3.3 or 5.0		V
VCC_{ripple} (Vin)	VCC ripple peak-to-peak		50	100	mV
V_{bat}	Battery voltage INPUT	1.3		5.5	V
V_{disp}	Display voltage OUTPUT		3.3		V
I_{Vdisp}	Vdisp current			20	mA
V_{cam}	Camera voltage OUTPUT		3.3		V
I_{Vcam}	Vcam current			20	mA
V_{IO}	I/O voltage OUTPUT		3.3		V
I_{VIO}	VIO current			20	mA
$V_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
$I_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED current			60	mA
$V_{VCC\_RGMII\_OUT}$	Supply voltage output for external PHY IO voltage		3.3V		V
$I_{VCC\_RGMII\_OUT}$	VCC_RGMII_OUT current			100	mA
$I_{operate}$	operating current (without V*_OUT pins, VCC = 3.3V)		450		mA
$P_{operate}$ (Power)	core module power consumption		1.5		W
IVbat	Vbat input current			5	mA
IVbat_Stby	Vbat Standby input current		800	1000	nA
VIH_3V3	Digital input high voltage	2.0	3.3		V
VIL_3V3	Digital input low voltage		0	0.8	V

Table 26: DC operating conditions

5.2 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
RESET_IN	System Reset input assertion time (active low)	10			ms
RESET_OUT	System Reset output assertion time (active low)	10			ms

Table 27: Reset Timings

5.3 Dimensions

Notes:

- Figure 10 shows an example with 5,2mm SODIMM-200 socket height.
- Figure 10 doesn't consider DHCOM-X (Molex High Speed Connector) socket.

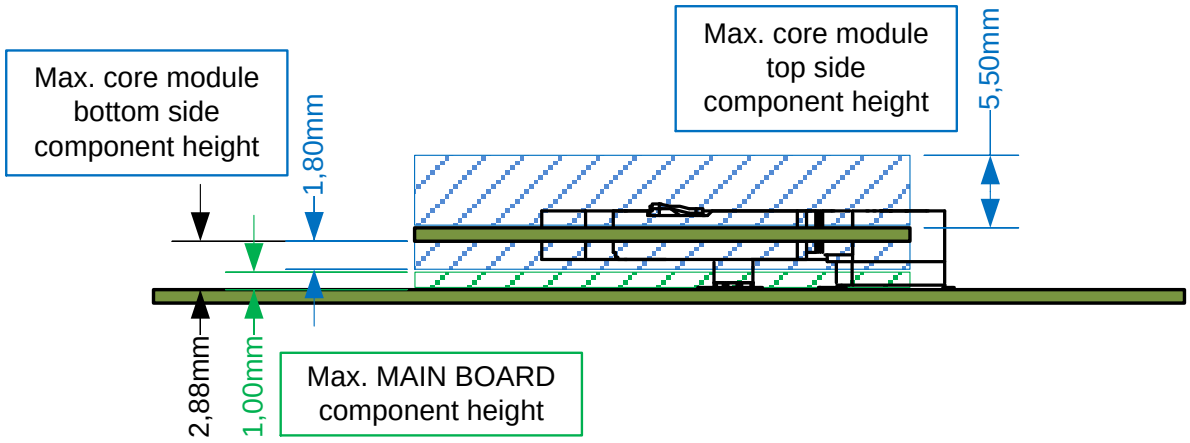

Figure 10: Maximum component heights

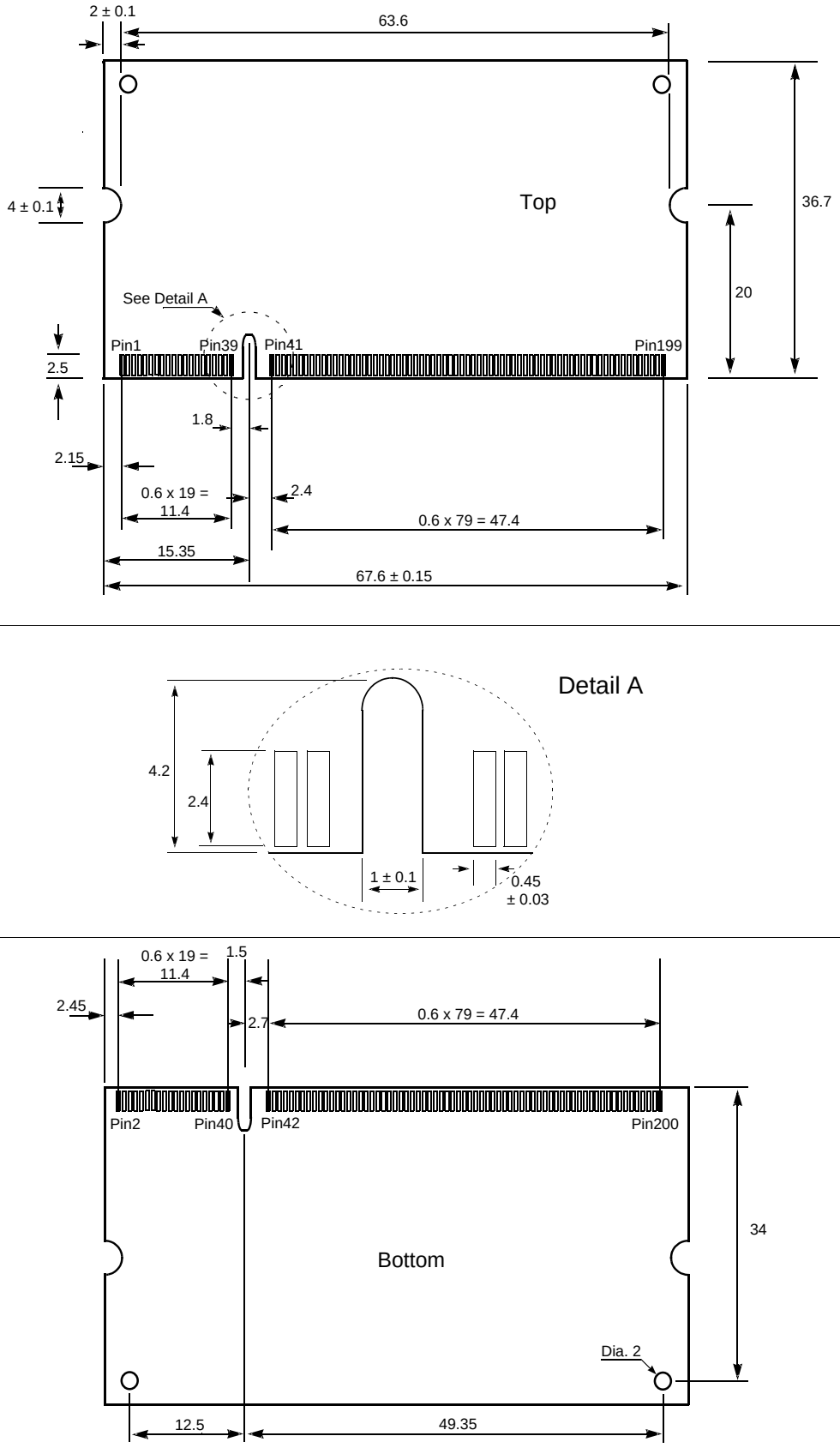

Figure 11: Dimensions of the module

5.4 Mechanical system

Several suggestions are given for the plugs, sockets and cables in the following subsections.

5.4.1 SODIMM-200 socket

The DHCM-AM335x module is designed for operation in a standard 2.5V (DDR) SODIMM-200 memory socket.

DHCOM-X note: DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector.

The following sockets have been successfully tested with the module:

Manufacturer	Description	Article number
Nexus Components http://www.nexus-de.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	DMD-200-RSE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	1473005-1
Nexus Components http://www.nexus-de.com/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	DMD-200-RPE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	1612618-1

Table 28: SODIMM-200 sockets

5.4.2 DHCOM-X (Molex High Speed Connector)

A Molex (http://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector. DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

SODIMM-200 socket height	Description	Article number
5.2mm	0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits	Molex 53748-0808
9.2mm	Not available	Not available

Table 29: DHCOM-X (Molex High Speed Connector)

5.4.3 JTAG FFC cable

Manufacturer	Description	Article number
Würth Elektronik http://www.we-online.com	▪ 0.50 mm flat flexible cable Type 1 WR-FPC	687 610 050 002
Molex http://www.molex.com/	▪ 0.50mm flat flexible cable Type A	982660097

Table 30: FFC Cable

5.5 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C

Table 31: Temperature range

6 RoHS conformance

This device has been manufactured RoHS compliant.