DHCOR STM32MP1

User Manual

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1   Changes

Version	Date	Changes	Name
R01	2019-05-02	First draft	AG
R02	2019-08-07	First official release	AG
R03	2019-08-14	Added SD-Card boot	AG
R04	2019-10-15	Added Hardware design checklist	AG
R05	2019-12-12	Added eMMC connection Added thermal example	AG
R05	2019-12-12	Released	HH

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3 Abbreviations

- ANA = Analog
- BGA = Ball grid array
- EMC = Electro magnetic compatibility
- ESD = electrostatic discharge
- HW = Hardware
- I/O = Input/output
- LGA = Land grid array
- MBC = Must be connected
- MSL = Moisture sensitivity level
- NC = No connect
- PD = Pull-down
- PnP = Pick and place
- PU = Pull-up
- RFU = Reserve for Future Use
- RST = Reset
- SAC = SnAgCu (Tin-silver-copper)
- SMT = Surface mounted technology
- SSU = Should stay connected
- SWD = Serial wire debug
- TBD = To be defined
- VSF = Vendor specific function

4   Introduction

4.1   Hardware

The DHCOR-STM32MP1-01LG is the second module in our solderable computer module series with a size of 29 x 29 mm². The space-saving module increases operational safety through direct soldering and saves space- and cost-intensive board-to-board connectors. The DHCOR STM32MP1 can be equipped with processors of the new STM32MP1 family and connects a Cortex-M4 processor (209 MHz) with one or two Cortex-A7 cores (650 MHz).

The module from the STM32MP1 family provides many embedded interfaces such as two 16 bit ADCs, 12 bit DACs, PWM/Timer, 148 GPIO, UART, SPI, RTC, up to 2x FD CAN and standard features like I2S, I2C™, GBit Ethernet , 8, 10 or 14 Bit camera interface, SD/MMC and one each USB 2.0 High Speed OTG and host port. The display interface is a 24 bit RGB or Mipi-DSI connection with HD resolution (1366 x 768 pixels). The optional integrated Vivante 3D GPU runs at up to 533 MHz clock speed, supports Open GL ES 2.0 and is feasible for powerful graphical user interfaces.

The DHCOR STM32MP1 is perfectly suited for many fields of application and sets itself apart from the masses with its diverse analogue and digital capabilities. The STM32MP1 family enables powerful IoT and/or HMI applications from sensors and actuators to the cloud with just one chip.

4.2 Software

Currently, the DHCOR-STM32MP1-01LG module is available with the Embedded Linux operating system based on Debian distribution or Yocto based.

4.3 Main characteristics

- Dual Cortex®-A7 up to 650 MHz and single Cortex®-M4 up to 209 MHz
- 3D GPU OpenGL ES2.0 up to 533 MHz
- Absolutely power efficient and cost optimized application processor
- Power management: STPMIC1A
- Crypto Engine, Secure Boot
- Quad SPI boot flash: 2 MByte
- DDR3 memory (32 bit): 256 - 1024 MByte
- Bus interface: 8 / 16 Bit address / data
- Ethernet: 1x Gbit, IEEE 1588, 1x MDIO
- MMC/SD: 3x SDIO 3.0 / SD 3.0 / eMMC 4.51
- NAND: 8 / 16 Bit interface Raw MLC / SLC, 8 Bit ECC

- Quad SPI: Dual Quad SPI

- CAN: 2x FDCAN / TTCAN

- UART: 4x UART, 4x USART up to 12.5 MBit/s

- SPI: 6x up to 50 MBit/s

- I2C™: 6x

- USB Host: 2x USB 2.0 HS

- USB OTG: 1x OTG 2.0 FS / HS

- Embedded USB PHYs: 2x HS + 1x FS

- CSI (parallel camera): 1x 8, 10 or 14 Bit / pixel data format

- Display RGB: Max. 1366 x 768 pixels, 24 Bit

- MIPI®-DSI: 2x data lanes (max. 1366 x 768 pixels)

- HDMI-CEC: 1x

- ADC: 2x 16-Bit synchronized / up to 22 channels

- DAC: Internal 1.5 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input

- Temperature sensor: 1x

- SPDIF: 4x Tx and Rx

- I2S / SAI: 4x

- GPIOs: 148x

- PWM / Timer: 2x 16 Bit motor control PWM synchronized AC timer, 10x 16 Bit timer, 5x 16 bit LP timer, 2x 32 Bit timer

- RTC: Secure RTC

- DFSDM: 1x with 8 channels / 6 filters

- Debug interface: JTAG interface

- Industrial temperature range (-40°C to +85°C)

4.4 Further technical information

Beside this manual, please also have a look at the ST application note **AN5031 "Getting started with STM32MP1 Series hardware development"**. This document shows how to use the STM32MP1 series and describes the minimum hardware resources required to develop a carrier board based on those MPU products.

For more precise technical information regarding STM32MP1 processor or PMIC1A power manager, please check the websites of the chip manufacturer: https://www.st.com

5   Hardware overview

5.1   Block diagram
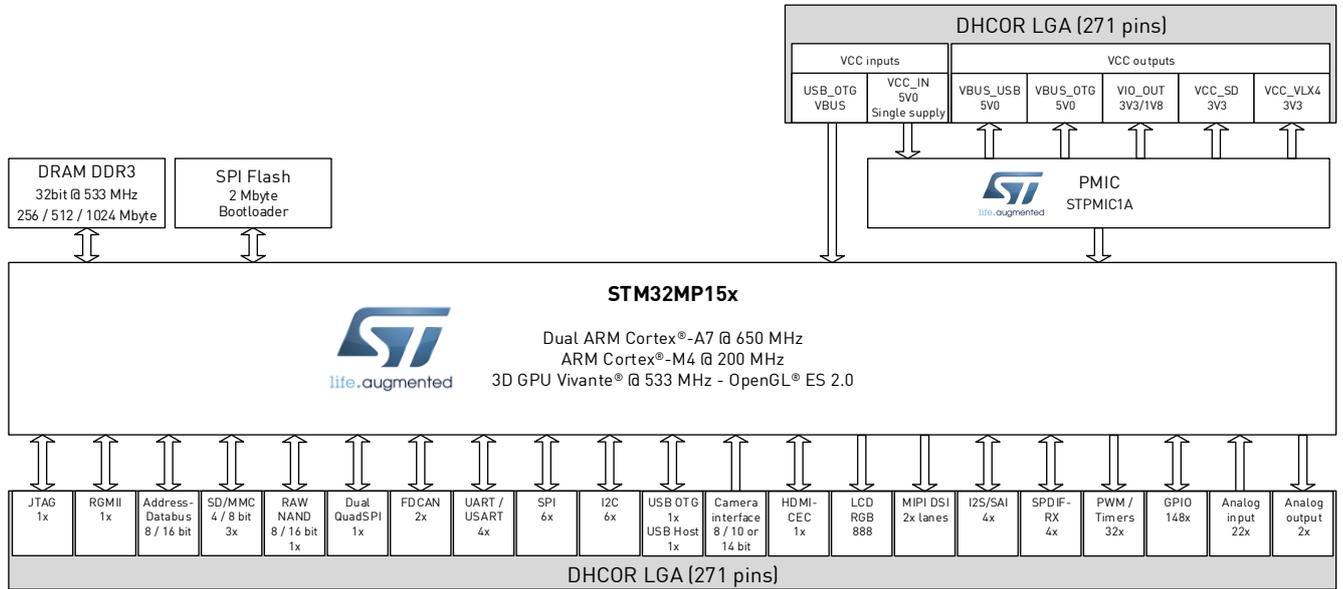
Figure 1: DHCOR-STM32MP1-01LG block diagram

5.2   Avenger96: Reference design

The reference design for DHCOR STM32MP1 is the Avenger96 Board:

https://wiki.dh-electronics.com/index.php/Avenger96

https://www.96boards.org/product/avenger96/

Important: It is recommended to reuse the DHCOR pin assignment of the Avenger96 as far as possible in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can be taken from the Avenger96, without any BSP porting efforts.

5.3   Pin assignment

The DHCOR-STM32MP1-01LG comes with the CPU type STM32MP15xxAC3 and with 12 x 12 mm TFBGA361 package.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec-tions on DHCOR	Pin not used
VCC_IO	1V8 or 3V3	A2	PWR	Output	-	-	-	-
VCC_IO	1V8 or 3V3	A3	PWR	Output	-	-	-	-
PA11	FDCAN1_RX	A4	GPIO	I/O	PA11	AA18	-	-

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connections on DHCOR	Pin not used
VBUS_SW[1]	USB_H_VBUS	A5	PWR	Output	-	-	-	-
GND	GND	A6	PWR	-	-	-	-	MBC
VBUS_OTG[2]	USB_OTG_VBUS	A7	PWR	Output	-	-	-	-
PF9_QSPI_BK1_IO1	QSPI_BK1_IO1	A8	GPIO	I/O	PF9	AA14	Connected to SPI flash	-
PF8_QSPI_BK1_IO0	QSPI_BK1_IO0	A9	GPIO	I/O	PF8	AC11	Connected to SPI flash	-
VCC_IN_5V	5V supply voltage	A10	PWR	Input	-	-	-	MBC
VCC_IN_5V	5V supply voltage	A11	PWR	Input	-	-	-	MBC
PD1	UART4_TX	A12	GPIO	I/O	PD1	B9	-	-
PB5	FDCAN2_RX	A13	GPIO	I/O	PB5	Y8	-	-
PD11	SAI2_SD_A	A14	GPIO	I/O	PD11	AC10	-	-
PF14	I2C1_SCL	A15	GPIO	I/O	PF14	AC4	-	-
GND	GND	A16	PWR	-	-	-	-	MBC
VCC_LDO6[3]	1V0	A17	PWR	Output	-	-	-	-
PA7	ETH1_RGMII_RX_CTL	A18	GPIO	I/O	PA7	AB8	-	-
PC2	ETH1_RGMII_TXD2	A19	GPIO	I/O	PC2	Y2	-	-
PG14	ETH1_RGMII_TXD1	A20	GPIO	I/O	PG14	AA1	-	-
PE2	ETH1_RGMII_TXD3	A21	GPIO	I/O	PE2	Y1	-	-
GND	GND	B1	PWR	-	-	-	-	MBC
VCC_IO	1V8 or 3V3	B2	PWR	Output	-	-	-	-
VCC_IO	1V8 or 3V3	B3	PWR	Output	-	-	-	-
PA12	FDCAN1_TX	B4	GPIO	I/O	PA12	AB19	-	-
VBUS_SW[4]	USB_H_VBUS	B5	PWR	Output	-	-	-	-
GND	GND	B6	PWR	-	-	-	-	MBC
VBUS_OTG[5]	USB_OTG_VBUS	B7	PWR	Output	-	-	-	-
PB6_QSPI_BK1_CS#	QUADSPI_BK1_NCS	B8	GPIO	I/O	PB6	Y14	10k PU to VCC_IO and con. to SPI flash	-
PF7_QSPI_BK1_IO2	QUADSPI_BK1_IO2	B9	GPIO	I/O	PF7	AB12	Connected to SPI flash	-
VCC_IN_5V	5V supply voltage	B10	PWR	Input	-	-	-	MBC
VCC_IN_5V	5V supply voltage	B11	PWR	Input	-	-	-	MBC
PB2	UART4_RX	B12	GPIO	I/O	PB2	Y16	-	-
PB13	FDCAN2_TX	B13	GPIO	I/O	PB13	AA10	-	-
PF11	SAI2_SD_B	B14	GPIO	I/O	PF11	Y10	-	-
PC0	SAI2_FS_B	B15	GPIO	I/O	PC0	AB5	-	-
PF12	ADC1_INP6	B16	GPIO	I/O	PF12	Y9	-	-
PF13	ADC2_INP2	B17	GPIO	I/O	PF13	Y5	-	-
PG11	ETH1_RGMII_TX_CTL	B18	GPIO	I/O	PG11	Y7	-	-
PC4	ETH1_RGMII_RXD0	B19	GPIO	I/O	PC4	AC7	-	-

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[1] These pins are connected to STPMIC1A Pin 38. USB Host power output switch (500mA or 1000mA). For more information see STPMIC1A datasheet.

[2] These pins are connected to STPMIC1A Pin 35. USB OTG power output switch. For more information see STPMIC1A datasheet.

[3] These pins are connected to STPMIC1A Pin 21. LDO6 (default voltage 1V0 / not turned ON automatically). For more information see STPMIC1A datasheet.

[4] These pins are connected to STPMIC1A Pin 38. USB Host power output switch. For more information see STPMIC1A datasheet.

[5] These pins are connected to STPMIC1A Pin 35. USB OTG power output switch. For more information see STPMIC1A datasheet.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec- tions on DHCOR	Pin not used
PC1	ETH1_MDC	B20	GPIO	I/O	PC1	AA6	-	-
PG4	ETH1_RGMII_GTX_CLK	B21	GPIO	I/O	PG4	AB2	-	-
GND	GND	C1	PWR	-	-	-	-	MBC
VCC_BUCK4[6]	3V3	C2	PWR	Output	-	-	-	-
VCC_BUCK4[6]	3V3	C3	PWR	Output	-	-	-	-
GND	GND	C4	PWR	-	-	-	-	MBC
USBH_HS1_DP	USB_DP1	C5	USB	Analog	USB_DP1	AC17	-	-
GND	GND	C6	PWR	-	-	-	-	MBC
USB_OTG_HS_VBUS	OTG_VBUS	C7	USB	Analog	OTG_VBUS	AC19	-	-
USB_OTG_HS_DP	USB_DP2	C8	USB	Analog	USB_DP2	AC16	-	-
PF6_QSPI_BK1_IO3	QUADSPI_BK1_IO3	C9	GPIO	I/O	PF6	AA13	Connected to SPI flash	-
VCC_IN_5V	5V supply voltage	C10	PWR	Input	-	-	-	MBC
VCC_IN_5V	5V supply voltage	C11	PWR	Input	-	-	-	MBC
PE8	UART7_TX	C12	GPIO	I/O	PE8	AC13	-	-
PE9	UART7_RTS	C13	GPIO	I/O	PE9	AA9	-	-
PD13	SAI2_SCK_A	C14	GPIO	I/O	PD13	AA19	-	-
PF15	I2C1_SDA	C15	GPIO	I/O	PF15	Y4	-	-
GND	GND	C16	PWR	-	-	-	-	MBC
GND	GND	C17	PWR	-	-	-	-	MBC
PC5	ETH1_RGMII_RXD1	C18	GPIO	I/O	PC5	AB7	-	-
PB12	ETH1_RGMII_TXD0	C19	GPIO	I/O	PB12	AC5	-	-
PA1	ETH1_RGMII_RX_CLK	C20	GPIO	I/O	PA1	AA4	-	-
PA2	ETH1_MDIO	C21	GPIO	I/O	PA2	AC3	-	-
GND	GND	D1	PWR	-	-	-	-	MBC
VCC_BUCK4[7]	3V3	D2	PWR	Output	-	-	-	-
VCC_BUCK4[7]	3V3	D3	PWR	Output	-	-	-	-
GND	GND	D4	PWR	-	-	-	-	MBC
USBH_HS1_DM	USB_DM1	D5	USB	Analog	USB_DM1	AB17	-	-
GND	GND	D6	PWR	-	-	-	-	MBC
PA10	OTG_ID	D7	GPIO	I/O	PA10	Y17	-	-
USB_OTG_HS_DM	USB_DM2	D8	USB	Analog	USB_DM2	AB16	-	-
PF10_QSPI_BK1_CLK[8]	QUADSPI_CLK	D9	GPIO	I/O	PF10	Y12	22R ser. resistor and connected to SPI flash	-
VCC_IN_5V	5V supply voltage	D10	PWR	Input	-	-	-	MBC
VCC_IN_5V	5V supply voltage	D11	PWR	Input	-	-	-	MBC
PE10	UART7_CTS	D12	GPIO	I/O	PE10	Y15	-	-
PE7	UART7_RX	D13	GPIO	I/O	PE7	AA11	-	-
PD12	SAI2_FS_A	D14	GPIO	I/O	PD12	Y18	-	-
PH2	SAI2_SCK_B	D15	GPIO	I/O	PH2	AB4	-	-
GND	GND	D16	PWR	-	-	-	-	MBC

[6] These pins are connected to STPMIC1A Pin 27. BUCK4 (default voltage 3V3 / turned ON automatically). For more information see STPMIC1A datasheet.

[7] These pins are connected to STPMIC1A Pin 27. BUCK4 (default voltage 3V3 / turned ON automatically). For more information see STPMIC1A datasheet.

[8] Note: 22R series resistance included between CPU and DHCOR ball.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec- tions on DHCOR	Pin not used
GND	GND	D17	PWR	-	-	-	-	MBC
PH6	ETH1_RGMII_RXD2	D18	GPIO	I/O	PH6	Y11	-	-
PB1	ETH1_RGMII_RXD3	D19	GPIO	I/O	PB1	AA7	-	-
PG5	ETH1_RGMII_CLK125	D20	GPIO	I/O	PG5	Y6	-	-
VCC_LDO2[9]	1V8	D21	PWR	Output	-	-	-	-
BOOT2	BOOT2	E1	BOOT	Input	BOOT2	M2	-	MBC
BOOT1	BOOT1	E2	BOOT	Input	BOOT1	N4	-	MBC
BOOT0	BOOT0	E3	BOOT	Input	BOOT0	N1	-	MBC
PONKEY#[10]	PONKEY#	E4	GPIO	Input	-	-	Connected to PMIC	-
PMIC_WAKEUP[11]	WKUP3	F1	GPIO	I/O	PC13	K2	Connected to PMIC	-
VBAT	VBAT	F2	PWR	Input	VBAT	1F1	-	VCC_IO
PA0_SYS_WKUP1	WKUP1	F3	GPIO	I/O	PA0	AB3	-	-
ANA1	ADC1_INP1	F4	ANA	Input	ANA1	U4	-	-
RST#	NRST	G1	RST	I/O	NRST	M3	4k7 PU to VCC_IO, 100nF to GND and con. To PMIC	Add 10nF to GND
PA13	MCO1	G2	GPIO	I/O	PA13	N2	-	-
NC	Not connected	G3	-	-	-	-	-	-
ANA0	ADC1_INP0	G4	ANA	Input	ANA0	U3	-	-
NC	Not connected	H1	-	-	-	-	-	-
NC	Not connected	H2	-	-	-	-	-	-
NC	Not connected	H3	-	-	-	-	-	-
NC	Not connected	H4	-	-	-	-	-	-
NC	Not connected	J1	-	-	-	-	-	-
NC	Not connected	J2	-	-	-	-	-	-
NC	Not connected	J3	-	-	-	-	-	-
NC	Not connected	J4	-	-	-	-	-	-
NC	Not connected	K1	-	-	-	-	-	-
NC	Not connected	K2	-	-	-	-	-	-
NC	Not connected	K3	-	-	-	-	-	-
NC	Not connected	K4	-	-	-	-	-	-
NC	Not connected	L1	-	-	-	-	-	-
NC	Not connected	L2	-	-	-	-	-	-
NC	Not connected	L3	-	-	-	-	-	-
NC	Not connected	L4	-	-	-	-	-	-
NC	Not connected	M1	-	-	-	-	-	-
NC	Not connected	M2	-	-	-	-	-	-
NC	Not connected	M3	-	-	-	-	-	-
NC	Not connected	M4	-	-	-	-	-	-
NC	Not connected	N1	-	-	-	-	-	-
NC	Not connected	N2	-	-	-	-	-	-
NC	Not connected	N3	-	-	-	-	-	-
NC	Not connected	N4	-	-	-	-	-	-

[9] These pins are connected to STPMIC1A Pin 18. LDO2 (default voltage 1V8 / not turned ON automatically). For more information see STPMIC1A datasheet.

[10] Connected to STPMIC1A Pin 17. User Power ON Key (active low with internal pullup).

[11] This pin is also connected to STPMIC1A Pin 2. Power ON from host processor (active high with internal pull-down).

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec- tions on DHCOR	Pin not used
NC	Not connected	P1	-	-	-	-	-	-
NC	Not connected	P2	-	-	-	-	-	-
NC	Not connected	P3	-	-	-	-	-	-
NC	Not connected	P4	-	-	-	-	-	-
GND	GND	R1	PWR	-	-	-	-	MBC
GND	GND	R2	PWR	-	-	-	-	MBC
GND	GND	R3	PWR	-	-	-	-	MBC
GND	GND	R4	PWR	-	-	-	-	MBC
NC	Not connected	T1	-	-	-	-	-	-
NC	Not connected	T2	-	-	-	-	-	-
NC	Not connected	T3	-	-	-	-	-	-
SYS_JTRST	NJTRST	T4	JTAG	Input	NJTRST	B19	-	-
SYS_JTDO-SW0	JTDO-TRACESW0	U1	JTAG	Output	JTDO-TRACE-SW0	A19	-	-
SYS_JTDI	JTDI	U2	JTAG	I/O	JTDI	A20	-	-
SYS_JTCK-SWCLK	JTCK-SWCLK	U3	JTAG	Input	JTCK-SWCLK	B20	-	-
SYS_JTMS-SWDIO	JTMS-SWDIO	U4	JTAG	I/O	JTMS-SWDIO	C20	-	-
PZ7	GPIO: HW Code bit 0	E18	GPIO	I/O	PZ7	J3	10k PU to VCC_IO or PD to GND	-
PG0	GPIO: RAM Code bit 0	E19	GPIO	I/O	PG0	AC2	10k PU to VCC_IO or PD to GND	-
PB11	GPIO	E20	GPIO	I/O	PB11	AB1	-	-
PG1	GPIO: RAM Code bit 1	E21	GPIO	I/O	PG1	W1	10k PU to VCC_IO or PD to GND	-
PC3	GPIO	F18	GPIO	I/O	PC3	W2	-	-
PG2[12]	GPIO: CSI_ERROR	F19	GPIO	I/O	PG2	V2	-	-
PF3	GPIO: HW Code bit 1	F20	GPIO	I/O	PF3	U1	10k PU to VCC_IO or PD to GND	-
PA14	GPIO	F21	GPIO	I/O	PA14	T2	-	-
PI5[13]	GPIO: SD_SEL	G18	GPIO	I/O	PI5	F3	-	-
PD8	GPIO	G19	GPIO	I/O	PD8	K3	-	-
PD14	GPIO	G20	GPIO	I/O	PD14	L3	-	-
PG3[14]	GPIO: CSI_INT	G21	GPIO	I/O	PG3	T3	-	-
PZ3[15]	GPIO: WIFI_LED	H18	GPIO	I/O	PZ3	T4	-	-
PD15	GPIO	H19	GPIO	I/O	PD15	J2	-	-
PZ6[15]	GPIO: BT_LED	H20	GPIO	I/O	PZ6	H1	-	-
PZ1[16]	GPIO: ETH1_INT	H21	GPIO	I/O	PZ1	G1	-	-
PZ2[16]	GPIO: ETH1_RST	J18	GPIO	I/O	PZ2	J4	-	-
PI8[13]	GPIO: SD_CD	J19	GPIO	I/O	PI8	L4	-	-

[12] Used for MIPI CSI bridge error input on Avenger96 board.
[13] Used for SD card control on Avenger96 board.
[14] Used for MIPI CSI bridge control on Avenger96 board.
[15] Used for LED connection on Avenger96 board.
[16] Used for Ethernet control on Avenger96 board.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec-tions on DHCOR	Pin not used
PG9[17]	GPIO: HDMI_INT	J20	GPIO	I/O	PG9	Y13	-	-
PF1	I2C2_SCL	J21	GPIO	I/O	PF1	A5	-	-
PH5	I2C2_SDA	K18	GPIO	I/O	PH5	A2	-	-
PZ0[14]	GPIO: CSI_XSDN	K19	GPIO	I/O	PZ0	G3	-	-
PZ5_I2C4_SDA	I2C4_SDA	K20	GPIO	I/O	PZ5	H2	1.5k PU to VCC_IO and con. To PMIC	-
PZ4_I2C4_SCL	I2C4_SCL	K21	GPIO	I/O	PZ4	G2	1.5k PU to VCC_IO and con. To PMIC	-
PD3	USART2_CTS	L18	GPIO	I/O	PD3	D14	-	-
PF5	USART2_TX	L19	GPIO	I/O	PF5	D7	-	-
PD4	USART2_RTS	L20	GPIO	I/O	PD4	B6	-	-
PD6	USART2_RX	L21	GPIO	I/O	PD6	D2	-	-
PB10	SPI2_SCK	M18	GPIO	I/O	PB10	Y3	-	-
PI3	SPI2_MOSI	M19	GPIO	I/O	PI3	E1	-	-
PI2	SPI2_MISO	M20	GPIO	I/O	PI2	E2	-	-
PI0	SPI2_NSS	M21	GPIO	I/O	PI0	C1	-	-
GND	GND	N18	PWR	-	-	-	-	MBC
GND	GND	N19	PWR	-	-	-	-	MBC
GND	GND	N20	PWR	-	-	-	-	MBC
GND	GND	N21	PWR	-	-	-	-	MBC
NC	Not connected	P18	-	-	-	-	-	-
NC	Not connected	P19	-	-	-	-	-	-
NC	Not connected	P20	-	-	-	-	-	-
NC	Not connected	P21	-	-	-	-	-	-
PG10	LCD_B2	R18	GPIO	I/O	PG10	AB11	-	-
PB0	LCD_G1	R19	GPIO	I/O	PB0	AB6	-	-
PA3	LCD_B5	R20	GPIO	I/O	PA3	U2	-	-
PG13	LCD_R0	R21	GPIO	I/O	PG13	AA2	-	-
PG7	LCD_CLK	T18	GPIO	I/O	PG7	AC14	-	-
PG8	LCD_G7	T19	GPIO	I/O	PG8	AB9	-	-
PH3	LCD_R1	T20	GPIO	I/O	PH3	AA3	-	-
PI10	LCD_HSYNC	T21	GPIO	I/O	PI10	T1	-	-
PB8	LCD_B6	U18	GPIO	I/O	PB8	AB10	-	-
PI11	LCD_G6	U19	GPIO	I/O	PI11	P4	-	-
PA5	LCD_R4	U20	GPIO	I/O	PA5	V3	-	-
PD9	LCD_B0	U21	GPIO	I/O	PD9	K1	-	-
GND	GND	V1	PWR	-	-	-	-	MBC
NC	Not connected	V2	-	-	-	-	-	-
DSI_CK_P	DSI_CKP	V3	DSI	Analog	DSI_CKP	B16	-	-
DSI_D0_P	DSI_D0P	V4	DSI	Analog	DSI_D0P	C15	-	-
PD2	SDMMC1_CMD	V5	GPIO	I/O	PD2	D12	-	-
PC12	SDMMC1_CK	V6	GPIO	I/O	PC12	D13	-	-
NC	Not connected	V7	-	-	-	-	-	-
NC	Not connected	V8	-	-	-	-	-	-
PC6	SDMMC2_D6	V9	GPIO	I/O	PC6	B14	-	-

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[17] Used for HDMI control on Avenger96 board.

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec-tions on DHCOR	Pin not used
PB14	SDMMC2_D0	V10	GPIO	I/O	PB14	C13	-	-
PD7	SDMMC3_D3	V11	GPIO	I/O	PD7	D10	-	-
PF0	SDMMC3_D0	V12	GPIO	I/O	PF0	D8	-	-
NC	Not connected	V13	-	-	-	-	-	-
PA6	DCMI_PIXCLK	V14	GPIO	I/O	PA6	AC8	-	-
PH7	DCMI_D9	V15	GPIO	I/O	PH7	W4	-	-
PE6	DCMI_D7	V16	GPIO	I/O	PE6	C10	-	-
PI6	DCMI_D6	V17	GPIO	I/O	PI6	F4	-	-
PG12	LCD_B1	V18	GPIO	I/O	PG12	K4	-	-
PI9	LCD_VSYNC	V19	GPIO	I/O	PI9	H4	-	-
PE12	LCD_B4	V20	GPIO	I/O	PE12	B4	-	-
PI7	LCD_B7	V21	GPIO	I/O	PI7	F2	-	-
NC	Not connected	W1	-	-	-	-	-	-
NC	Not connected	W2	-	-	-	-	-	-
DSI_CK_N	DSI_CKN	W3	DSI	Analog	DSI_CKN	A16	-	-
DSI_D0_N	DSI_D0N	W4	DSI	Analog	DSI_D0N	B15	-	-
PC10	SDMMC1_D2	W5	GPIO	I/O	PC10	D15	-	-
PC8	SDMMC1_D0	W6	GPIO	I/O	PC8	D18	-	-
NC	Not connected	W7	-	-	-	-	-	-
NC	Not connected	W8	-	-	-	-	-	-
PB3	SDMMC2_D2	W9	GPIO	I/O	PB3	A11	-	-
PB15	SDMMC2_D1	W10	GPIO	I/O	PB15	B12	-	-
PA15	SDMMC2_D5	W11	GPIO	I/O	PA15	C19	-	-
PF4	SDMMC3_D1	W12	GPIO	I/O	PF4	D9	-	-
NC	Not connected	W13	-	-	-	-	-	-
NC	Not connected	W14	-	-	-	-	-	-
PA4	DCMI_HSYNC	W15	GPIO	I/O	PA4	V4	-	-
PE1	DCMI_D3	W16	GPIO	I/O	PE1	C8	-	-
PI1	DCMI_D8	W17	GPIO	I/O	PI1	E3	-	-
PH9	LCD_R3	W18	GPIO	I/O	PH9	C5	-	-
PH8	LCD_R2	W19	GPIO	I/O	PH8	D5	-	-
PE15	LCD_R7	W20	GPIO	I/O	PE15	D3	-	-
PH13	LCD_G2	W21	GPIO	I/O	PH13	D1	-	-
NC	Not connected	Y1	-	-	-	-	-	-
NC	Not connected	Y2	-	-	-	-	-	-
DSI_D1_N	DSI_D1N	Y3	DSI	Analog	DSI_D1N	A17	-	-
PC11	SDMMC1_D3	Y4	GPIO	I/O	PC11	D16	-	-
PC9	SDMMC1_D1	Y5	GPIO	I/O	PC9	D17	-	-
PB9	SDMMC1_CDIR	Y6	GPIO	I/O	PB9	B10	-	-
GND	GND	Y7	PWR	-	-	-	-	MBC
GND	GND	Y8	PWR	-	-	-	-	MBC
PA8	SDMMC2_D4	Y9	GPIO	I/O	PA8	A13	-	-
PC7	SDMMC2_D7	Y10	GPIO	I/O	PC7	B11	-	-
PD0	SDMMC3_CMD	Y11	GPIO	I/O	PD0	B8	-	-
PE3	SDMMC2_CK	Y12	GPIO	I/O	PE3	C9	-	-
NC	Not connected	Y13	-	-	-	-	-	-
NC	Not connected	Y14	-	-	-	-	-	-

DHCOR pad name	DHCOR default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Special connec- tions on DHCOR	Pin not used
PI4	DCMI_D5	Y15	GPIO	I/O	PI4	E4	-	-
PE0	DCMI_D2	Y16	GPIO	I/O	PE0	D6	-	-
PH14	DCMI_D4	Y17	GPIO	I/O	PH14	C3	-	-
PH4	LCD_G5	Y18	GPIO	I/O	PH4	B3	-	-
PH11	LCD_R5	Y19	GPIO	I/O	PH11	C4	-	-
PH12	LCD_R6	Y20	GPIO	I/O	PH12	B2	-	-
PH15	LCD_G4	Y21	GPIO	I/O	PH15	B1	-	-
NC	Not connected	AA1	-	-	-	-	-	-
NC	Not connected	AA2	-	-	-	-	-	-
DSI_D1_P	DSI_D1P	AA3	DSI	Analog	DSI_D1P	B17	-	-
PE4	SDMMC1_CKIN	AA4	GPIO	I/O	PE4	D19	-	-
PF2	SDMMC1_D0DIR	AA5	GPIO	I/O	PF2	A14	-	-
PE14	SDMMC1_D123DIR	AA6	GPIO	I/O	PE14	C6	-	-
VCC_SD_LDO5[18]	2V9 (SD card voltage)	AA7	PWR	Output	-	-	-	-
VCC_SD_LDO5[18]	2V9 (SD card voltage)	AA8	PWR	Output	-	-	-	-
PG6	SDMMC2_CMD	AA9	GPIO	I/O	PG6	A10	-	-
PB4	SDMMC2_D3	AA10	GPIO	I/O	PB4	B13	-	-
PG15	SDMMC3_CK	AA11	GPIO	I/O	PG15	B7	-	-
PD5	SDMMC3_D2	AA12	GPIO	I/O	PD5	A7	-	-
GND	GND	AA13	PWR	-	-	-	-	MBC
NC	Not connected	AA14	-	-	-	-	-	-
PB7	DCMI_VSYNC	AA15	GPIO	I/O	PB7	D11	-	-
PA9	DCMI_D0	AA16	GPIO	I/O	PA9	A8	-	-
PH10	DCMI_D1	AA17	GPIO	I/O	PH10	C2	-	-
PE5	LCD_G0	AA18	GPIO	I/O	PE5	C11	-	-
PD10	LCD_B3	AA19	GPIO	I/O	PD10	B5	-	-
PE11	LCD_G3	AA20	GPIO	I/O	PE11	A4	-	-
PE13	LCD_DE	AA21	GPIO	I/O	PE13	A3	-	-

Table 1: Pin assignment

6 Protection circuits

The DHCOR STM32MP1 module does **NOT** contain any protection circuits (e.g. ESD protection). These must be provided from the carrier board.

7 Power supply

The DHCOR-STM32MP1-01LG must be powered by a single 5.0 V supply voltage on the VCC_IN_5V pins. All oth-er voltages are directly generated by the STPMIC1A and can also be used on the carrier board for the supply of

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[18] These pins are connected to STPMIC1A Pin 20. LDO5 (default voltage 2V9 / turned ON automatically) with max. output current of 350mA. For more information see STPMIC1A datasheet.

peripheral components (Ethernet PHY, eMMC, …). This enables a carrier board design with only one buck regulator for the 5.0 V DHCOR supply voltage.

Note: The power supply must be buffered with at least two 47uF capacitors on the carrier board.

Furthermore, the STPMIC1A provides two power switches to supply the USB sub-system of the carrier board. These outputs are also directly available on the DHCOR pins VBUS_SW and VBUS_OTG.

Summary: The single supply voltage of 5.0 V and the integrated power switches for USB can significantly reduce the efforts and costs of the carrier board.

Figure 2: Power supply overview
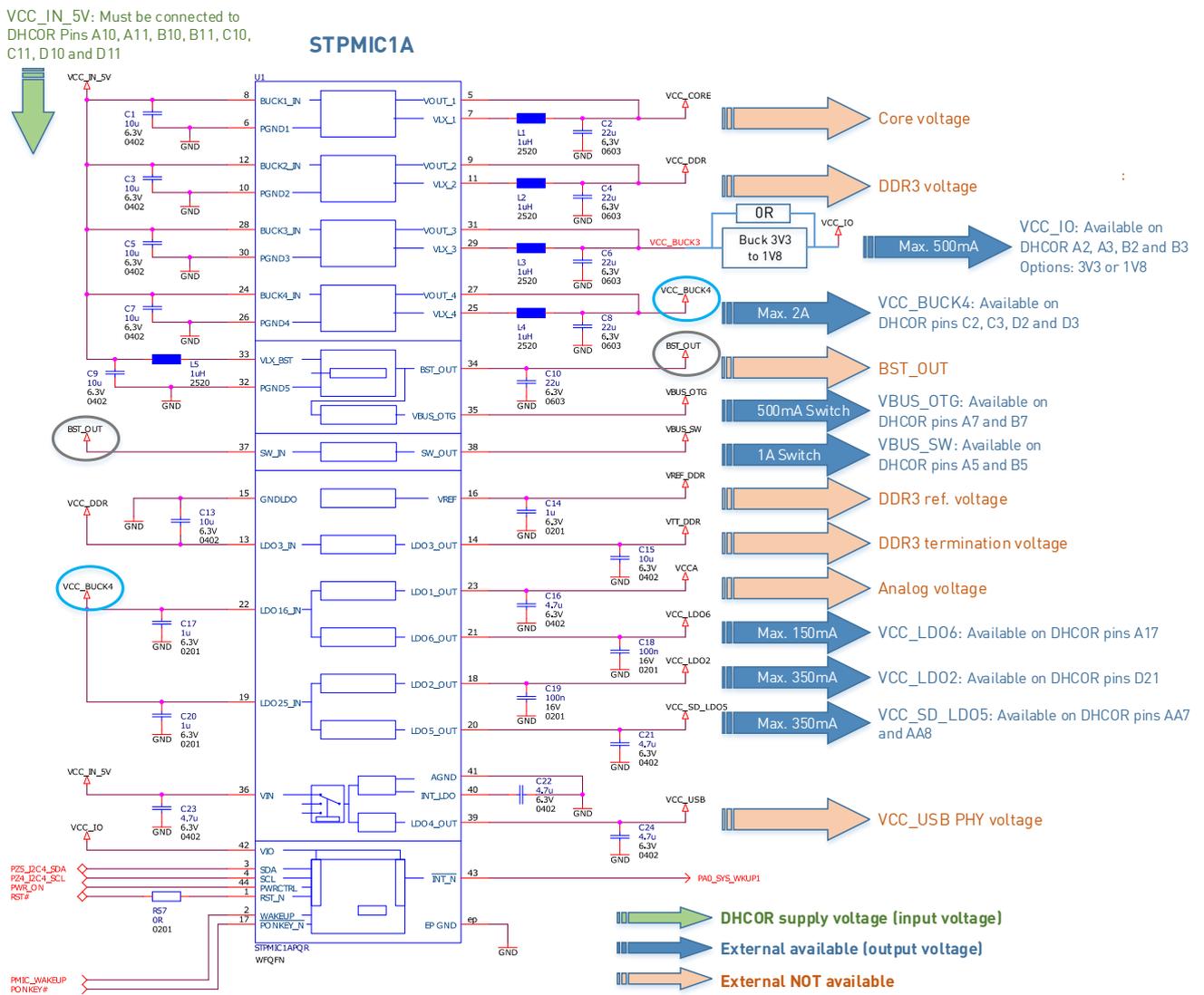
Notes:

- VCC_LDO2 and VCC_LDO6 are each buffered with a 100nF capacitor at the DHCOR module, because these regulators are unused at the module. This means that the customer has to add buffer capacitors to each of the regulators when they are used at the carrier board.
- When designing a carrier board, the EMC performance can be improved by adding filters to the supply voltages of the DHCOR module.
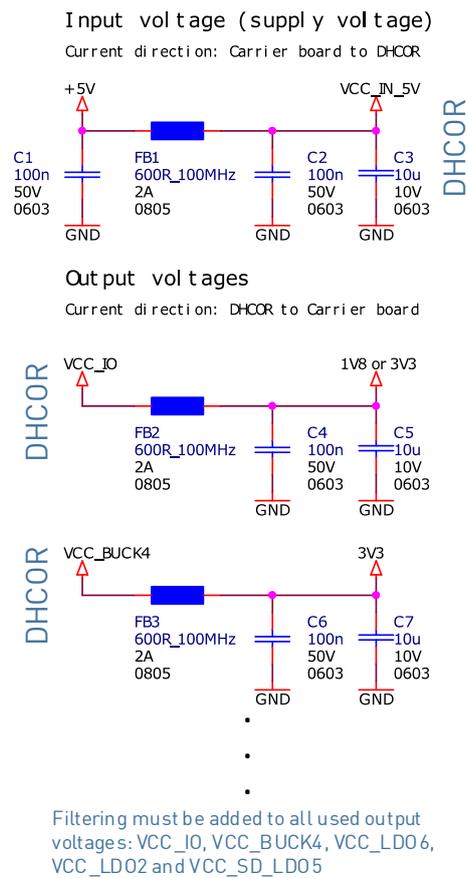
Figure 3: Power supply filtering

Filtering notes:

- Recommended ferrite: Wuerth 742792040 (maximum current of any supply voltage must be checked) or similar
- In case of USB (VBUS_OTG and VBUS_SW) no additional filtering is mentioned, because this is added with the standard USB schematic direct to the USB socket.

8   Reset

The reset signal RST# is active low and directly connected to the STM32MP1 NRST pin. VDD is connected to VCC_IO voltage.
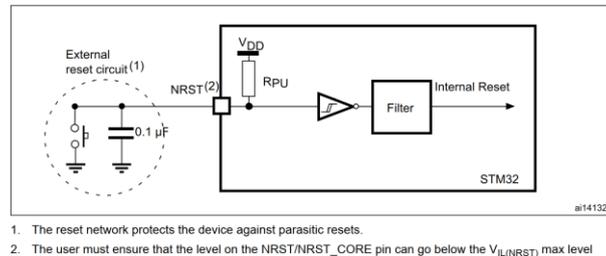
Figure 4: Reset

Notes: The 0.1µF capacitor is necessary, even if RST# is not used on the carrier board. It is also recommended to trigger a reset event (from the carrier board) only via an open-drain circuit. Do not connect RST# directly to VCC_IO.

For more precise technical information, we refer you to the ST reset documentation.

9   Boot modes

The STM32MP1 BOOT pins are directly available on the DHCOR pins E1, E2 and E3. The standard boot mode is serial NOR-Flash boot from the DHCOR Quad SPI Flash (on module). For this mode BOOT0 **MUST** be set on the carrier board to logical "1" via a 1k pull-up to VCC_IO and BOOT1, BOOT2 must be set to logical "0" via a direct connection to GND. It is also recommended to add an additional pull-down (not mounted) or debug switch (to GND) to BOOT0 to be able to enter UART and USB boot mode. For more precise technical information, we refer you to the ST boot mode documentation.

Note: No pull-up or pull-down resistors are added to the BOOT pins at the DHCOR module. These parts **MUST** be added external on the carrier board.

Beside NOR Flash boot the following boot modes are available:

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB[1]	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB High-Speed device on OTG_HS_DP/DM pins[2]
0	0	1	Serial NOR-Flash[3]	Serial NOR-Flash on QUADSPI[5]
0	1	0	eMMC™[3]	eMMC™ on SDMMC2 (default)[5][6]
0	1	1	NAND-Flash[3]	SLC NAND-Flash on FMC
1	0	0	Reserved	Used to get debug access without boot from Flash[4]
1	0	1	SD-Card[3]	SD-Card on SDMMC1 (default)[5][6]
1	1	0	UART and USB[1][3]	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB High-speed device on OTG_HS_DP/DM pins[2]
1	1	1	Serial NAND-Flash[3]	Serial NAND-Flash on QUADSPI[5]

1. Could be disabled by OTP settings.
2. USB requires 24 MHz HSE clock/crystal if OTP is not programmed for different frequency (See *Section 7.3: Embedded boot loader mode*).
3. Boot source could be changed by OTP settings (e.g. Initial boot on SD-Card, then eMMC with OTP settings).
4. Cortex-A7 Core0 in infinite loop toggling PA13, Cortex-M4 in infinite loop on RETRAM.
5. Default pins can be altered by OTP.
6. Alternatively, another SDMMC interface than this default can be selected by OTP.

Figure 5: Boot modes

9.1 SD-Card boot

If the carrier board contains a microSD/SD socket and it is planned to boot form microSD/SD card, it is mandatory to connect the card at the following CPU pins (otherwise SD-Card boot will not work):

- PC12: SDMMC1_CK
- PD2: SDMMC1_CMD
- PB9: SDMMC1_CDIR
- PC8: SDMMC1_D0

please also have a look at the ST application note AN5031 "**Getting started with STM32MP1 Series hardware development**".

Note: It is recommended to have microSD/SD socket available, because the board bring up is much easier with the possibility of SD-Card boot. If microSD/SD card is not needed during series production, the parts can stay unmounted.

10 Quad SPI NOR-Flash

The onboard Quad SPI NOR-Flash is connected to the QuadSPI interface bank1 of the STM32MP1. The used pins are also available on the DHCOR pins. It is possible to order the DHCOR module without onboard Quad SPI NOR-Flash as well. In that case the QuadSPI interface can be used on the carrier board without any limitations. In case the onboard Flash is mounted, it is recommended to left the pins open at the carrier board design, to ensure, that the CPU has full access to the Flash.

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
PB6_QSPI_BK1_CS#	QUADSPI_BK1_NCS	B8	GPIO	I/O	PB6	Y14	-
PF10_QSPI_BK1_CLK[19]	QUADSPI_CLK	D9	GPIO	I/O	PF10	Y12	-

[19] Note: 22R series resistance included between CPU and DHCOR ball.

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
PF8_QSPI_BK1_IO0	QSPI_BK1_IO0	A9	GPIO	I/O	PF8	AC11	-
PF6_QSPI_BK1_IO3	QUADSPI_BK1_IO3	C9	GPIO	I/O	PF6	AA13	-
PF7_QSPI_BK1_IO2	QUADSPI_BK1_IO2	B9	GPIO	I/O	PF7	AB12	-
PF9_QSPI_BK1_IO1	QSPI_BK1_IO1	A8	GPIO	I/O	PF9	AA14	-

Table 2: Quad SPI NOR-Flash signals

11 VBAT

The real-time clock (RTC) and backup registers can be supplied with the VBAT voltage when the main VCC_IO supply is powered off. This internal supply with automatic switch between VBAT and VCC_IO (VDD) is named VSW domain and is also used to supply PI8, PC13, PC14, PC15 pads. When VCC_IO is above VBAT, a small charging current could be enabled on VBAT for an external backup voltage device (e.g. supercapacitor). For details, please have a look at the ST documentation.

If no external battery is used in the application, it is required to connect VBAT externally to VCC_IO.

12 ADC / DAC reference voltage

The PMIC LDO1 (2.9 V) is connected, as external reference voltage, to the V_{REF+} pin of the STM32MP1 CPU. If it is necessary to use the internal reference voltage of the STM32MP1, please contact DH electronics for a special variant of DHCOR-STM32MP1-01LG.

13 I2C™

By default, the following STM32MP1 pins are used as I2C™ interface from DH electronics:

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
PF14	I2C1_SCL	A15	GPIO	I/O	PF14	AC4	-
PF15	I2C1_SDA	C15	GPIO	I/O	PF15	Y4	-
PF1	I2C2_SCL	J21	GPIO	I/O	PF1	A5	-
PH5	I2C2_SDA	K18	GPIO	I/O	PH5	A2	-
PZ5_I2C4_SDA	I2C4_SDA	K20	GPIO	I/O	PZ5	H2	-
PZ4_I2C4_SCL	I2C4_SCL	K21	GPIO	I/O	PZ4	G2	-

Table 3: I2C™ interface signals

Only I2C4 is fixed to the I2C™ functionality, because the PMIC STPMIC1A (I2C™ address: 0x33) is connected to this interface. Therefore, the pull-up resistors (1k5) to VCC_IO are located at the DHCOR module. For I2C1 and I2C2 no pull-up resistors are added to the signals on the DHCOR module. This means, the signals can be used for alternate functions as well.

14 Hardware and DDR3 coding

The following pins are used by DH electronics for hardware and DDR3 size coding:

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
PZ7	GPIO: HW Code bit 0	E18	GPIO	I/O	PZ7	J3	-
PF3	GPIO: HW Code bit 1	F20	GPIO	I/O	PF3	U1	-
PG0	GPIO: RAM Code bit 0	E19	GPIO	I/O	PG0	AC2	-
PG1	GPIO: RAM Code bit 1	E21	GPIO	I/O	PG1	W1	-

Table 4: Hardware and DDR3 coding pins

Hardware (PCB) version	PF3: HW Code bit 1	PZ7: HW Code bit 0
HW100 (version 1)	0	0
HW200 (version 2)	0	1
HW300 (version 3)	1	0
HW400 (version 4)	1	1

Table 5: Hardware coding

DDR3 size	PG1: RAM Code bit 1	PG0: RAM Code bit 0
128 Mbyte (not available)	0	0
256 MByte	0	1
512 MByte	1	0
1024 MByte	1	1

Table 6: DDR3 coding

Note:

- 1 = 10k pull-up at DHCOR module
- 0 = 10k pull-down at DHCOR module

Due to this the bootloader (U-Boot) scans the states of these pins during startup, starts the correct memory initialization and provides information regarding the PCB version in order to handle possible PCB differences correctly. The coding pins can be also used for alternate functions, but the customer must remove the pin scanning from bootloader and ensure the initialization of the DDR3 memory with the correct initialization values.

15 JTAG / SWD

The standard JTAG and SWD interface is directly available at the following DHCOR pins:

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
SYS_JTRST	NJTRST	T4	JTAG	Input	NJTRST	B19	-
SYS_JTDO-SWO	JTDO-TRACESWO	U1	JTAG	Output	JTDO-TRACESWO	A19	-
SYS_JTDI	JTDI	U2	JTAG	I/O	JTDI	A20	-
SYS_JTCK-SWCLK	JTCK-SWCLK	U3	JTAG	Input	JTCK-SWCLK	B20	-

DHCOR pad name	DH electronics default function	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball number	Not used
SYS_JTMS-SWDIO	JTMS-SWDIO	U4	JTAG	I/O	JTMS-SWDIO	C20	-

Table 7: JTAG / SWD pins

To avoid uncontrolled, I/O levels the STM32MP1 series embeds internal pull-up and pull-down resistors on the JTAG pins:

- SYS_JTRST: Internal pull-up

- SYS_JTDI: Internal pull-up

- SYS_JTDO-SWO: Internal pull-up

- SYS_JTMS-SWDIO: Internal pull-up

- SYS_JTCK-SWCLK: Internal pull-down

The next figure shows the connection between the STM32MP1 series and a standard JTAG/SWD connector:
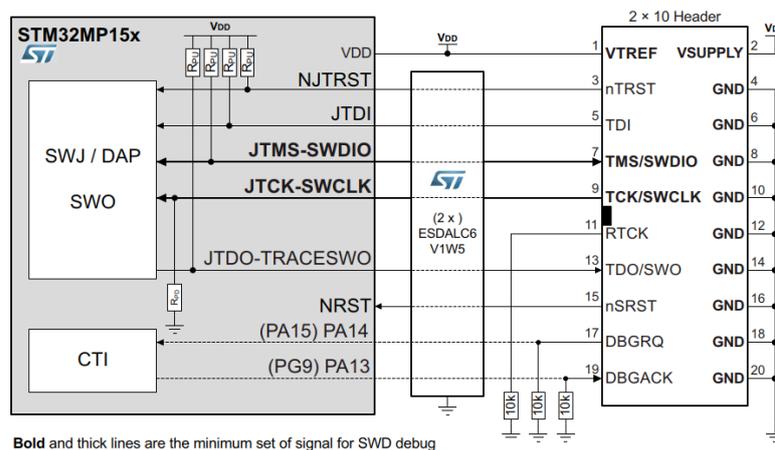
Figure 6: JTAG / SWD Connection

16 100Mbit Ethernet

The Avenger96 (see https://www.96boards.org/product/avenger96/) reference design implements a GBit Ethernet connection. This chapter shows how to connect an 100MBit PHY to the DHCOR-STM32MP1-01LG:

DHCOR pad name	DH electronics default function	100Mbit RMII signals	DHCOR pad	CPU ball name	CPU ball number
PA1	ETH1_RGMII_RX_CLK	ETH_CLK (50MHz ref. clock)	C20	PA1	AA4
PA7	ETH1_RGMII_RX_CTL	ETH1_RMII_CRS_DV	A18	PA7	AB8
PC4	ETH1_RGMII_RXD0	ETH1_RMII_RDX0	B19	PC4	AC7
PC5	ETH1_RGMII_RXD1	ETH1_RMII_RXD1	C18	PC5	AB7
PG11	ETH1_RGMII_TX_CTL	ETH1_RMII_TX_EN	B18	PG11	Y7
PB12	ETH1_RGMII_TXD0	ETH1_RMII_TXD0	C19	PB12	AC5

DHCOR pad name	DH electronics default function	100Mbit RMII signals	DHCOR pad	CPU ball name	CPU ball number
PG14	ETH1_RGMII_TXD1	ETH1_RMII_TXD1	A20	PG14	AA1
PC1	ETH1_MDC	ETH1_MDC	B20	PC1	AA6
PA2	ETH1_MDIO	ETH1_MDIO	C21	PA2	AC3
PZ1	GPIO: ETH1_INT	GPIO: ETH1_INT	H21	PZ1	G1
PZ2	GPIO: ETH1_RST	GPIO: ETH1_RST	J18	PZ2	J4
PC2	ETH1_RGMII_TXD2	*not required → freely usable*	A19	PC2	Y2
PE2	ETH1_RGMII_TXD3	*not required → freely usable*	A21	PE2	Y1
PH6	ETH1_RGMII_RXD2	*not required → freely usable*	D18	PH6	Y11
PB1	ETH1_RGMII_RXD3	*not required → freely usable*	D19	PB1	AA7
PG5	ETH1_RGMII_CLK125	*not required → freely usable*	D20	PG5	Y6

Table 8: Ethernet 100Mbit RMII signals

17 UART for bootloader and Linux console

It is strongly recommended to use one UART interface to enable access to the bootloader and linux console on the carrier board. The port can be deactivated during production to avoid illegal access to the series device, but for development and prototyping this port should be accessible.

On Avenger96 board, the following pins are used for bootloader and linux console:

- PD1: UART4_TX
- PB2: UART4_RX

18 USB OTG: Flash programming / STM32CubeProgrammer

It is strongly recommended to enable the access to the USB OTG port on the carrier board and the possibility to switch to UART and USB boot mode. Then STM32CubeProgrammer can be used to program any flash device supported on STM32MPU boards:

- microSD™ card
- eMMC
- NAND Flash memory
- NOR Flash memory

STM32CubeProgrammer is the official STMicroelectronics tool for creating partitions into any Flash device available on STM32 platforms. Once created, STM32CubeProgrammer allows populating and updating the partitions with the prebuilt binaries. The connection between the host PC and the board can be done through UART or USB serial links.
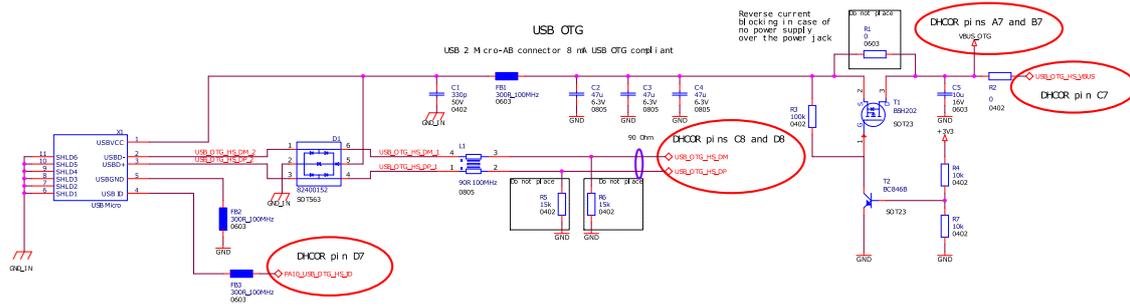
Figure 7: USB OTG

Note: Please ensure, that VBUS_OTG (DHCOR pins A7 and B7) is connected to USB_OTG_HS_VBUS (DHCOR pin C7)

19 eMMC connection

The external eMMC connection is a little bit tricky, because of the small eMMC housing pitch of 0.5 mm. But with the following instruction's it is possible to connect an eMMC with a standard 4-layer PCB with through hole vias and line width and spacing parameters of 0.120 mm. The main idea is to use unconnected pins for routing.

Note the following example is based on eMMC 5.1 JEDEC standard. Fortunately, the newer eMMC devices are backward compatible with the older eMMC specifications. The standard contains VSF, NC and RFU pins. The NC pins can be routed through while the RFU pins should be avoided during routing.
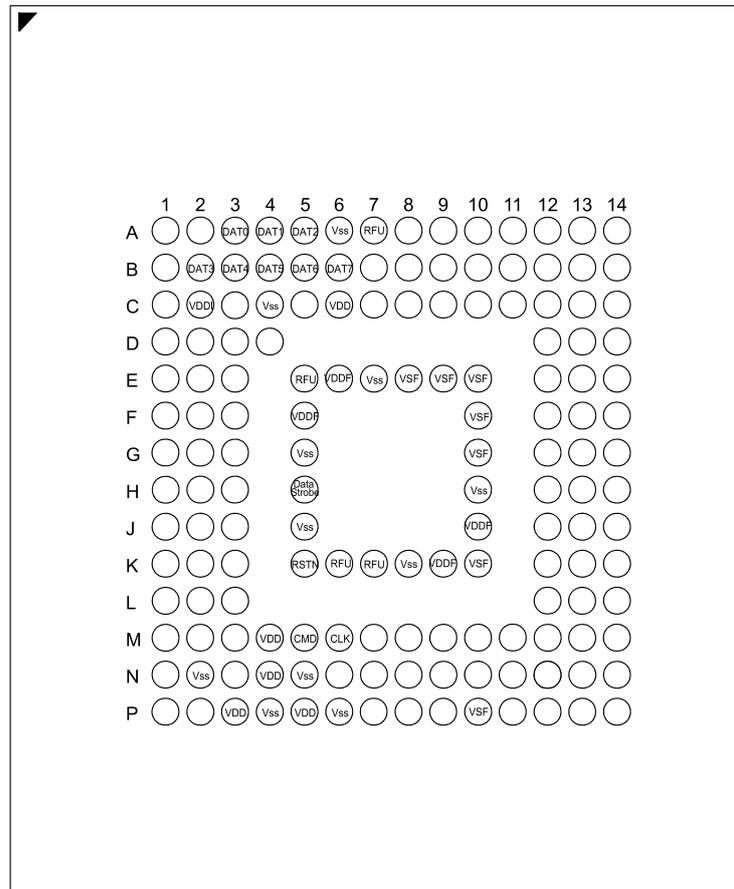
Figure 8: eMMC pinout (153 nall BGA), based on eMMC 5.1 JEDEC standard

Pin number	Name	Description
A3	DAT0	Bidirectional data channel DAT0
A4	DAT1	Bidirectional data channel DAT1
A5	DAT2	Bidirectional data channel DAT2
B2	DAT3	Bidirectional data channel DAT3
B3	DAT4	Bidirectional data channel DAT4
B4	DAT5	Bidirectional data channel DAT5
B5	DAT6	Bidirectional data channel DAT6
B6	DAT7	Bidirectional data channel DAT7
K5	RSTN	H/W reset signal pin
C6, M4, N4, P3, P5	VDD	Supply voltage for memory controller
E6, F5, J10, K9	VDDF	Supply voltage for flash memory
C2	VDDI	Internal power node to stabilize regulator output to controller core logics
M5	CMD	A bidirectional signal used for device initialization and command transfers.
H5	Data Strobe	Newly assigned pin for HS400 mode. Data Strobe is generated from e.MMC to host.
M6	CLK	Clock input
J5, A6, C4, E7, G5, H10, K8, N2, N5, P4, P6	VSS	Ground connections

Table 9: eMMC pin description

Figure 9 below shows the eMMC schematic example of DHCOR-STM32MP1-01LG connected to an eMMC v5.1 device. All of the reserved and additional pins are designated on the schematic symbol, only the not connected pins are left away, so it is easier to understand and avoid those pins in layout.
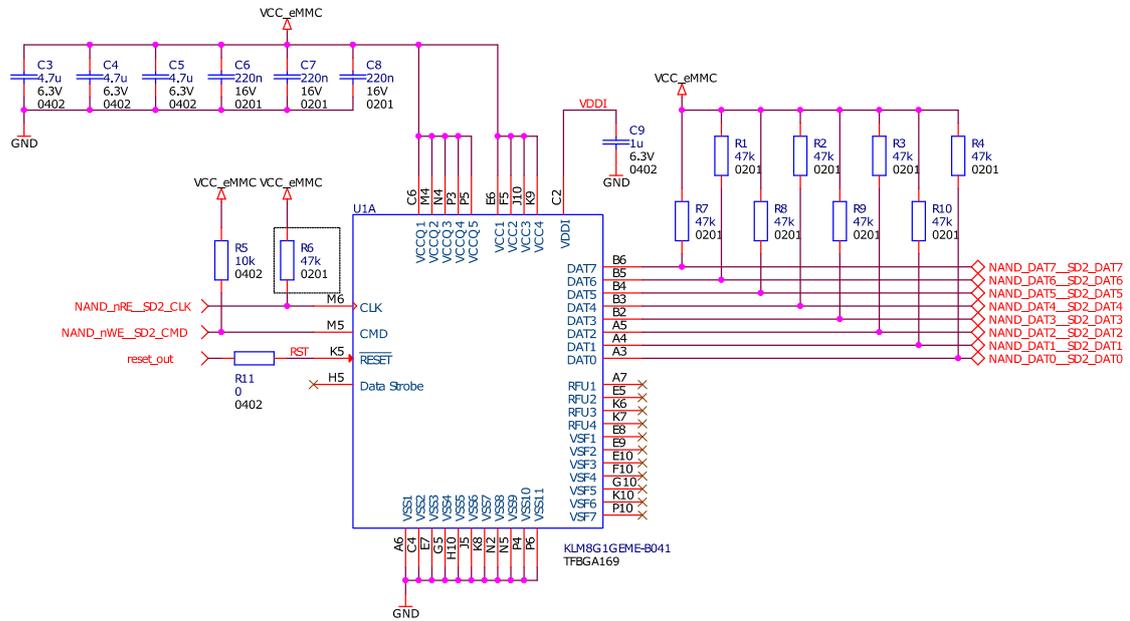
Figure 9: eMMC schematic example

Figure 10 shows an example routing of a v5.1 eMMC device using 0.12 mm trace / 0.12 mm space routing and 0.3 mm drill / 0.65 via pad.
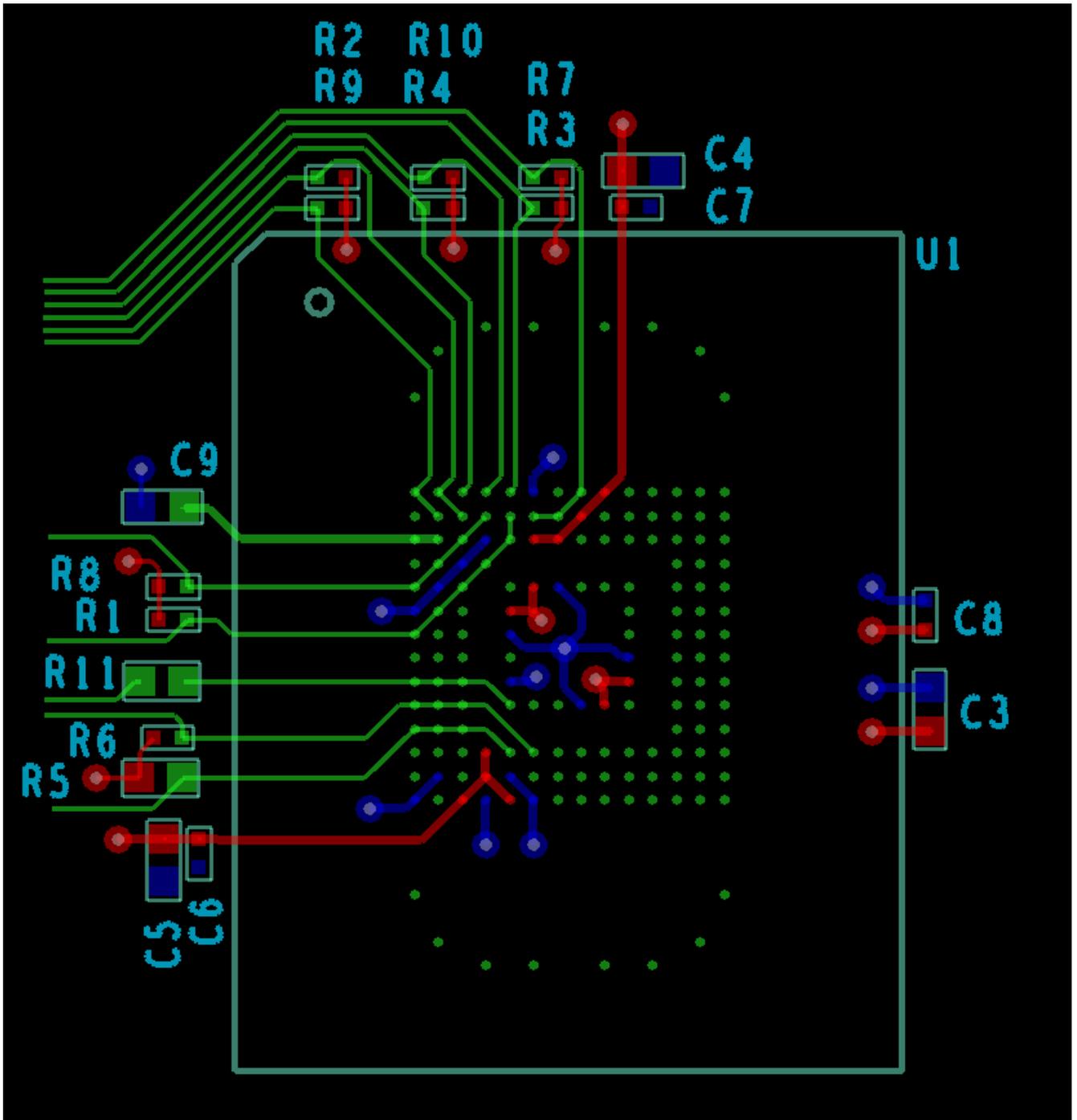
Figure 10: eMMC routing example

Note: The eMMC lines (CMD, CLK and DAT*) should be routed with matched trace lengths.

20 Technical specifications

20.1 Operating conditions – Absolute maximum / operating conditions

Symbol	Description	Input / Output	Min	Typ	Max	Unit
VCC_IN_5V	5V supply voltage	Input	4.2	5.0	5.5	V
$I_{VCC\_IN\_5V}$	Max. supply current	Input	Depends on max. used output power. See 20.2 for max. DHCOR power consumption.			
VCC_IN_5V$_{ripple}$	VCC ripple peak-to-peak	Input	-	30	60	mV
VBAT	Backup operating voltage	Input	1.2	-	3.6	V
I_{VBAT}	Max. backup current		-	-	1.35	mA
VCC_IO (V18 variant)	IO voltage	Output	-	1.8	-	V
$I_{VCC\_IO\ (V18\ variant)}$	Max. usable VCC_IO output current[20]	Output	-	-	400	mA
VCC_IO (V33 variant)	IO voltage	Output	-	3.3	-	V
$I_{VCC\_IO\ (V33\ variant)}$	Max. usable VCC_IO output current[20]	Output	-	-	400	mA
VCC_BUCK4	3V3 voltage	Output	-	3.3	-	V
I_{VCC_BUCK4}	Max. usable VCC_BUCK4 output current[20]	Output	-	-	800[21]	mA
VBUS_OTG	5V USB OTG power switch	Output	-	5.0	5.2	V
I_{VBUS_OTG}	Max. usable VBUS_OTG output current[20]	Output	-	-	500	mA
VBUS_SW	5V USB Host power switch	Output	-	5.0	5.2	V
I_{VBUS_SW}	Max. usable VBUS_SW output current[20]	Output	-	-	1000	mA
VCC_LDO2	LDO2 voltage	Output	1.7	1.8	3.3	V
I_{VCC_LDO2}	Max. usable VCC_LDO2 output current[20]	Output	-	-	350	mA
VCC_SD_LDO5	LDO5 SD card voltage	Output	1.7	2.9	3.9	V
$I_{VCC\_SD\_LDO5}$	Max. usable VCC_SD_LDO5 output current[20]	Output	-	-	350	mA
VCC_LDO6	LDO6 voltage	Output	0.9	1.0	3.3	V
I_{VCC_LDO6}	Max. usable VCC_LDO6 output current[20]	Output	-	-	150	mA
V_{IL}	I/O input low level voltage for VCC_IO = 1.8V	Input	-	-	0.35xVCC_IO	V
	I/O input low level voltage for VCC_IO = 3.3V	Input	-	-	0.3xVCC_IO	V
V_{IH}	I/O input high level voltage	Input	0.7xVCC_IO	-	-	V

Table 10: DC operating conditions

Note: The carrier board designer MUST always consider the thermal conditions on the DHCOR module.

20.2 DHCOR max. power consumption

Note: The values based on STM32MP157C core.

Symbol	Description	Power symbol	Max. power value
VCC_CORE	Digital core supply voltage	$P_{VCC\_CORE\_MAX}$	0,47 W (390 mA @ 1,2 V)
VCC_DDR	DDR3 supply voltage	$P_{VCC\_DDR\_MAX}$	0,68 W (500 mA @ 1,35 V)
VCC_BUCK3	IO supply voltage	$P_{VCC\_BUCK3\_MAX}$	0,33 W (100 mA @ 3,3 V)
VREF_DDR	DDR3 reference voltage	P_{VREF_DDR}	0,003 W (5 mA @ 0,675 V)

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[20] Maximum external (on carrier board) usable current from the supply output.

[21] The max. output current was reduced to 800 mA, because of thermal topics and the regulator is also used to supply LDO1, LDO2, LDO5 and LDO6.

Symbol	Description	Power symbol	Max. power value
VTT_DDR	DDR3 termination voltage	P_{VTT_DDR}	0,135 W (200 mA @ 0,675 V)
VCCA	Analog operation voltage	P_{VCCA}	Tbd (tbd @ 2,9 V)
VCC_USB	USB supply voltage	P_{VCC_USB}	Tbd (tbd @ 3,3 V)
Total DHCOR power consumption			1,618 W → Assumed max. **2 W** because of tbd values.

Table 11: DHCOR max. power consumption

20.3 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
RST#	System Reset input assertion time (active low)	350	-	-	ns
RST#	System Reset output assertion time (active low)	20	-	-	µs

Table 12: Reset Timings
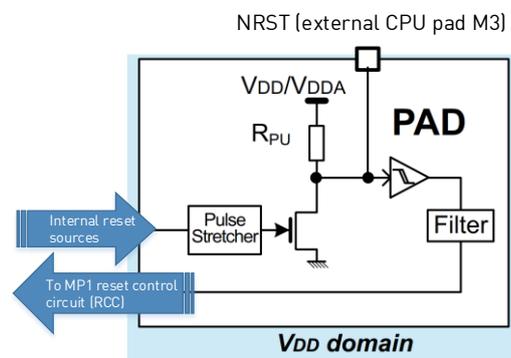
Figure 11: MP1 reset pad (MPU internal circuit)

20.4 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C

Table 13: Temperature range

Figure 12 shows the temperature conditions on the DHCOR STM32MP**157** (dual core with GPU) module under full load.

Test conditions:

- GPU Test: `glmark2-es2-wayland --run-forever --fullscreen > ~/test &`

- CPU stress test: `stress-ng --cpu 2 &`

- Memory test: `memtester 100 > /dev/null &`
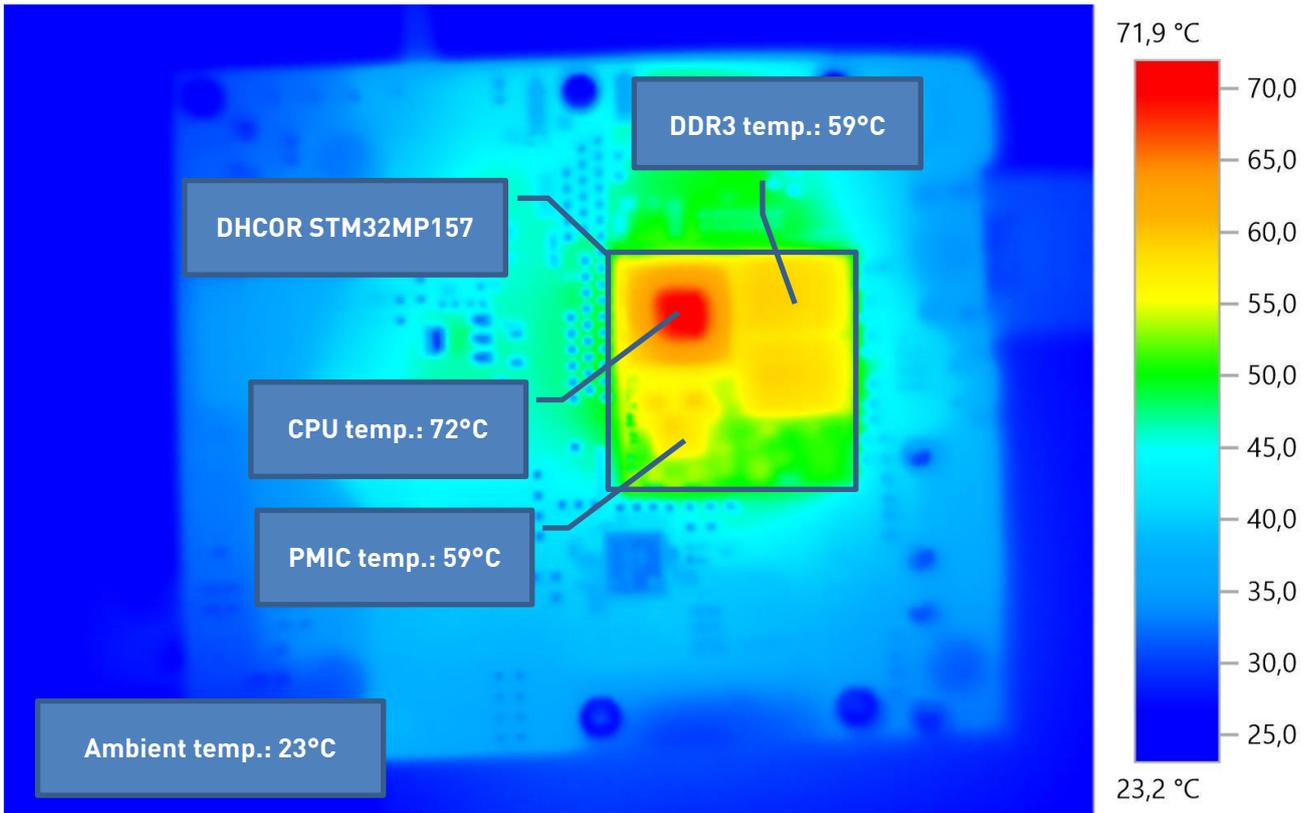
Figure 12: Temperature example (STM32MP157) at full load

# 21 Mechanical specifications

## 21.1 Dimensions
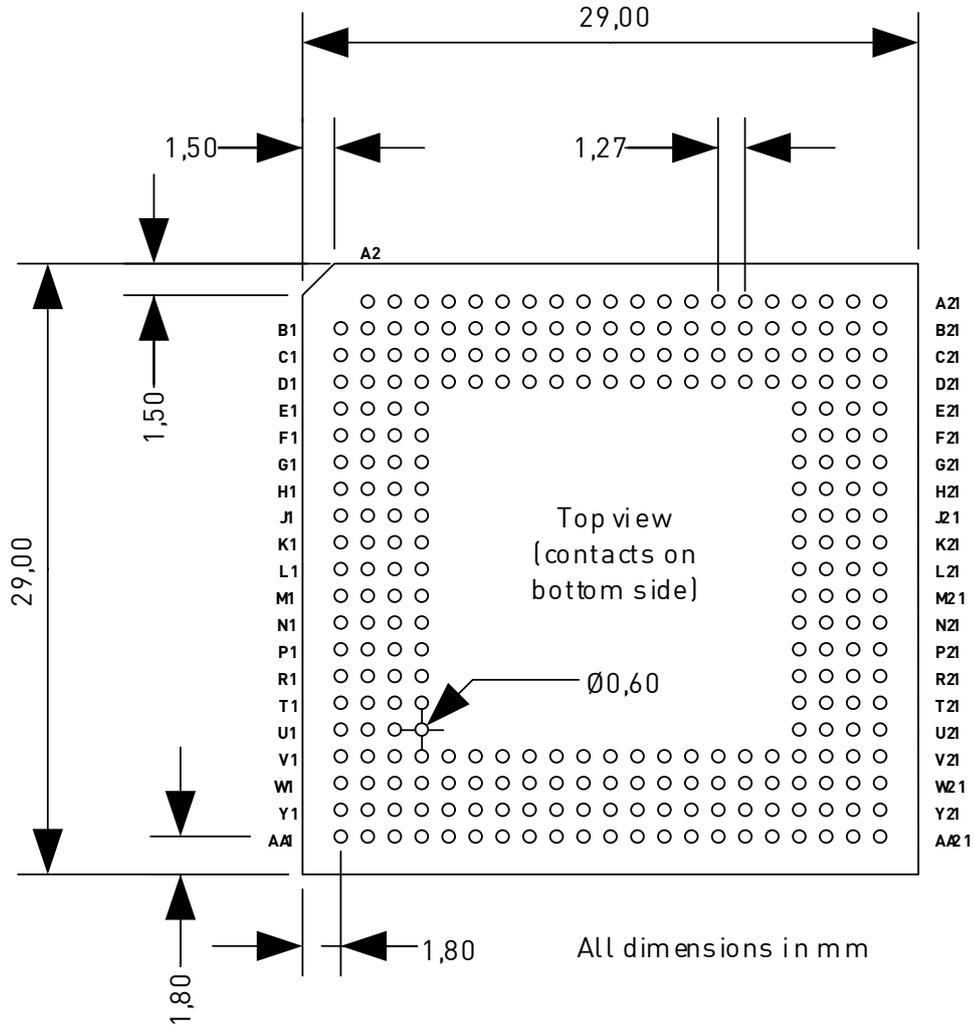
Figure 13: Dimensions of the module
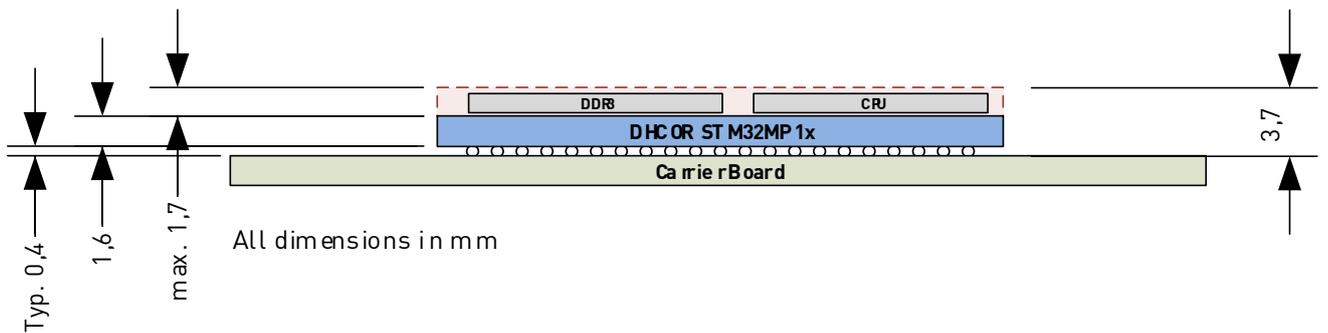
Figure 14: DHCOR height

21.2 PCB land pattern
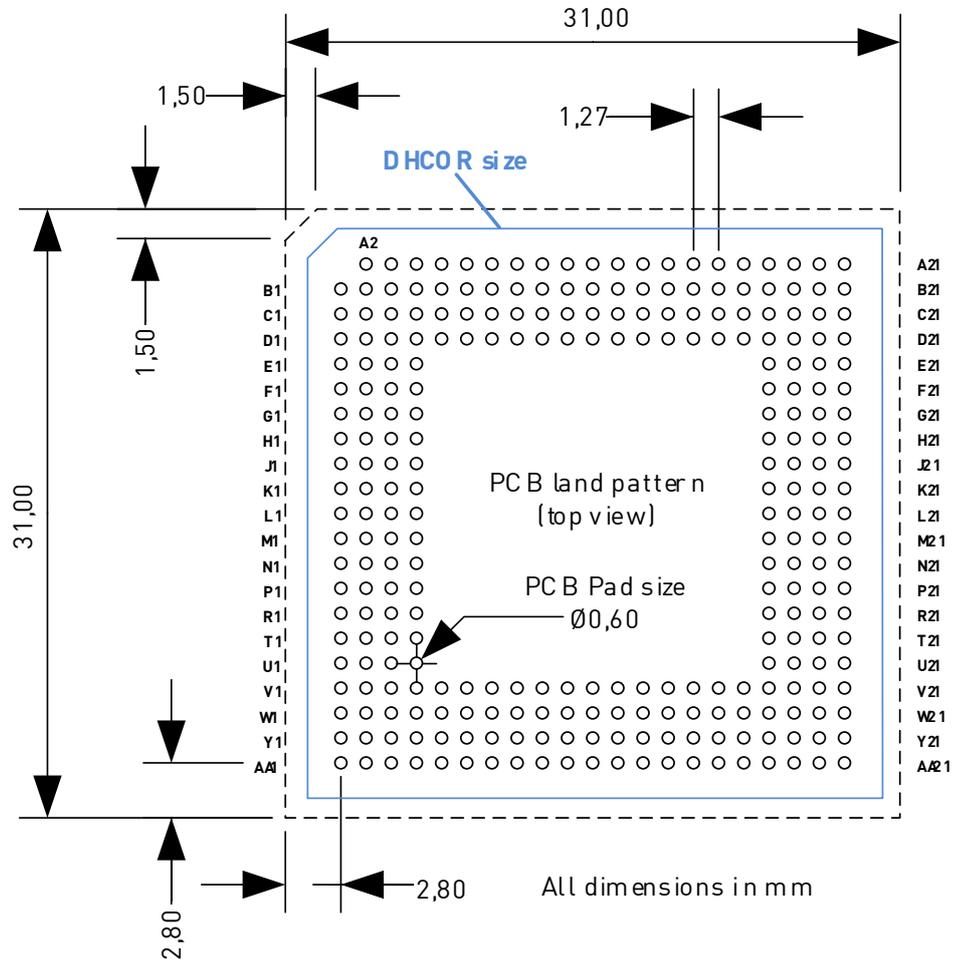
Figure 15: PCB land pattern

22 Assembly instructions

DHCOR-STM32MP1-01LG has been designed for SMT mounting of the module on the carrier board. The DHCOR uses LGA contact pads on the bottom side for the connection to the carrier board. During the production process of the module solder paste is applied to the LGA pads. Therefore, the DHCOR is nearly similar to a BGA. The solder paste on the pads improves the contact quality between module and carrier board, compared with a standard LGA part (without solder paste on the module pads).

22.1 Moisture sensitivity and shelf life

- Calculated shelf life in tape and real packaging: 12 months at < 40 °C and < 90 % relative humidity (RH).
- The DHCOR-STM32MP1-01LG is applicable to MSL3 (based on IPC/JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at < 30 °C and < 60 % RH and the product shall be used within 168 hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 $^{+5}/_{-0}$ °C, 24 hours, 1 time
- The products shall be baked on a heat-resistant tray since the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

22.2 Coplanarity

Coplanarity of the carrier board: < 0.1 mm

22.3 Solder pastes

Solder paste parameters:

- Any lead-free (Pb-free) SAC solder pastes can be used.

Solder paste print parameters:

- Stencil thickness: > 0.1 mm (recommended 0.15 mm)
- Stencil pad diameter: Suggestion 0.55 mm (0.6 mm pad size)

22.4 Reflow Process

Use reflow profiles per IPC/JEDEC J-STD-020D.

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.

Profile Feature	Pb-Free Assembly
Preheat	
- Temperature Min (T_{smin})	150 °C
- Temperature Max (T_{smax})	200 °C
- Time (t_L)	60-120 seconds
Time maintained above:	
- Temperature (T_L)	217 °C
- Time (t_L)	60-150 °C
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6°C/second max.
Time 25 °C to peak temperature	8 minutes max.

**Table 14: Reflow profil per IPC/JEDEC J-STD-020E**
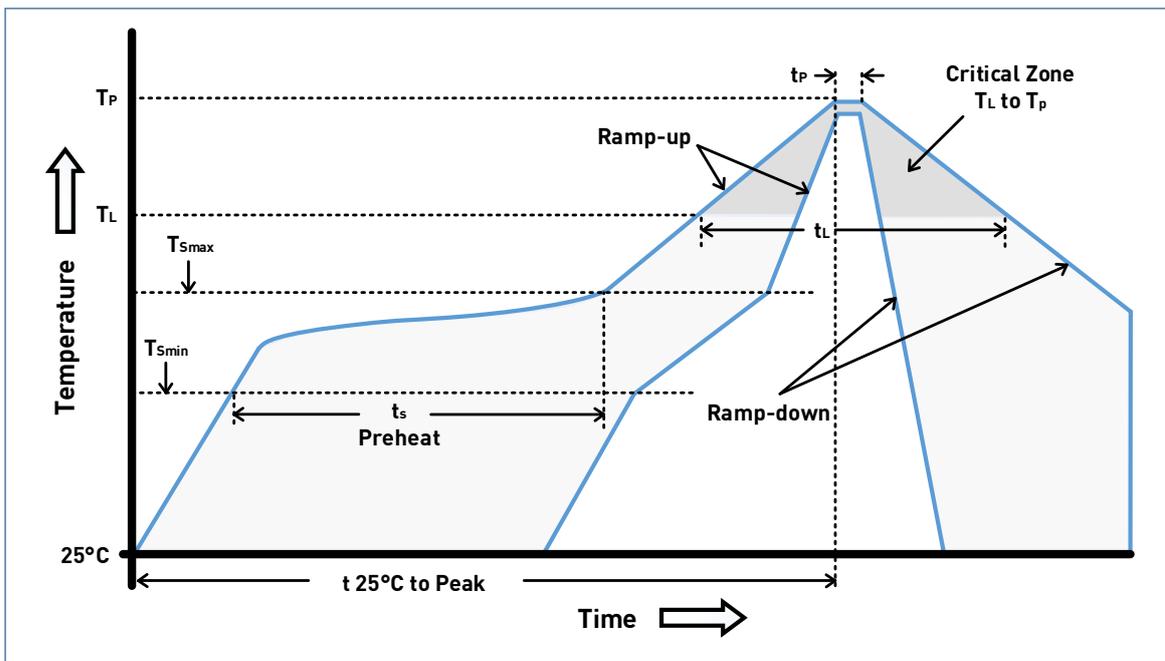
Figure 16: Reflow Classification Profile

The manufacturing of the DHCOR-STM32MP1-01LG requires two reflow cycles. Two reflow cycles are remaining for mounting the module on the carrier board. It is strongly recommended to solder the DHCOR-STM32MP1-01LG module during the last reflow cycle of the carrier board manufacturing process.

23 Tape and reel packaging
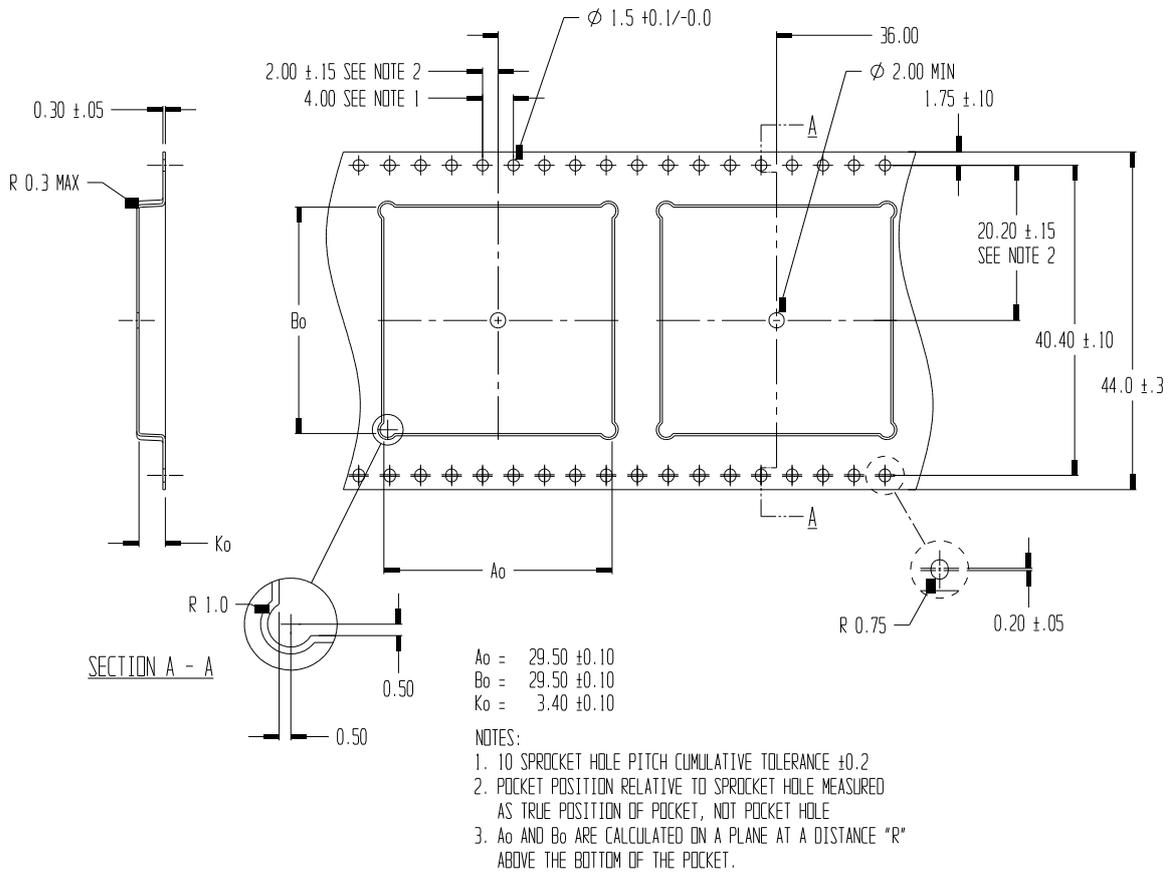
Figure 17: Tape and reel packaging

24 Hardware design checklist

Table 15 is a checklist for all the important design guidelines. Please read each checklist entry carefully to ensure that your carrier board design meets these guidelines.

Number	Checklist / Design notes
1	It is recommended to reuse the DHCOR pin assignment of the Avenger96 as far as possible in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can be taken from the Avenger96, without any BSP porting efforts. Please have a look at chapter 5.2 Avenger96: Reference design
2	Does the carrier board design provide any connection to the JTAG pins (e.g. mounting option, only for development)? Please have a look at chapter 15 JTAG / SWD

Number	Checklist / Design notes
3	Are the BOOT pins provided with correct pull-up or pull-down resistors for the preferred boot options? Please have a look at chapter 9 Boot modes
4	The easiest way for the board bring up is the microSD boot option. DH electronics recommended to have microSD/SD socket available on the carrier board. If microSD/SD card is not needed during series production, the parts can stay unmounted. Please have a look at chapter 9.1 SD-Card boot
5	DH electronics strongly recommends to enable the access to the USB OTG port on the carrier board for flash programming. Please have a look at chapter 18 USB OTG: Flash programming / STM32CubeProgrammer
6	Please ensure, that VBAT is connected to VCC_IO at the carrier board design, if no external battery is used in the application. Please have a look at chapter 11 VBAT
7	Ensure, that the Quad SPI NOR-Flash pins are left open at the carrier board design, if a DHCOR variant with Onboard SPI flash is used. Please have a look at chapter 10 Quad SPI NOR-Flash
8	If VCC_LDO2 or VCC_LDO6 are used on the carrier board (not used on DHCOR STM32MP1 module), the buffer capacitors must be added to the design. Please have a look at chapter 7 Power supply
9	Ensure correct RST# connection. Please have a look at chapter 8 Reset
10	Does the carrier board design provide any serial connection to bootloader and Linux console? Please have a look at chapter 17 UART for bootloader and Linux console

Table 15: Hardware design checklist

25 RoHS conformance

This device has been manufactured RoHS II-compliant.