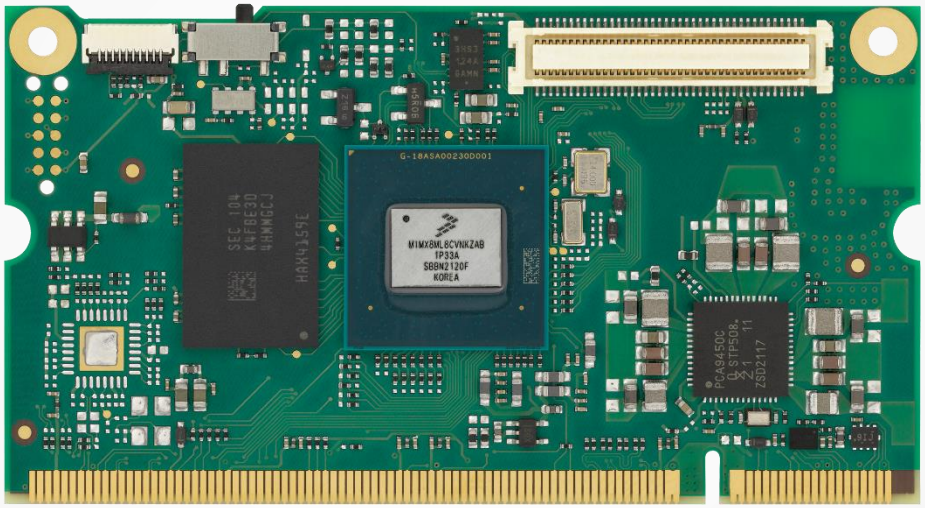
DHCOM i.MX8M Plus

User manual



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History

Version	Data	Description of changes	Name
R01	18.10.2022	First version	AG
R01	18.11.2022	Reviewed and released	MA

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Abbreviations

- ADC = Analog to Digital Converter
- AIN = Analog input
- AINOUT = Analog Input / Output
- BLE = Bluetooth low energy
- BR / EDR = Bluetooth basic rate / enhanced
- BSP = Board support packages
- ECC = error correcting code
- FFC = Flat flex cable
- GPIO = General Purpose Input / Output
- GPU = Graphics processing unit
- I = Input
- IO = Input / output
- LTS = Long term support
- MBC = Must be connected
- MIPI Alliance = Mobile Industry Processor Interface Alliance
- NPU = Neural processing unit
- O = Output
- PD = Pull-Down
- PHY = Physical layer
- PMIC = Power management IC
- PU = Pull-Up
- PWM = Pulse Width Modulation
- PWR_I = Power input
- PWR_O = Power output
- RGB = Red, green, and blue
- RTC = Real time clock
- SAI = Serial Audio Interface
- SBC = Should be connected
- SoC = System on chip
- SoM = System on module
- TBD = To be defined
- TCPC = Type-C port controller
- TSN = Time-sensitive networking

1 Introduction

1.1 Hardware

The DHCOM i.MX8M Plus SoM is based on the NXP® i.MX 8M Plus SoCs. The i.MX8M Plus Quad features four Cortex-A53 cores and a single Cortex-M7 co-processor. The main cores run at up to 1.8 GHz for commercial graded products and 1.6 GHz for industrial temperature range products. The Cortex-M7 supports a maximum speed of 800 MHz. This heterogeneous multicore system allows running additional real-time operating systems on the M7 cores for time- and security-critical tasks.

The high-end version of the i.MX8M Plus SoC features a Neural Processing Unit (NPU) with up to 2.3 TOPS that can speed up machine learning tasks. Next to this the SoC features inline error correcting code (ECC) for the LPDDR4 DRAM for high system reliability and safety. And the integrated Vivante® GC7000 UltraLite 3D Graphics Processing Unit (GPU), supports OpenGL® ES 3.0, OpenCL® 1.2, and Vulkan®.

The i.MX8M Plus features many embedded interfaces, like 2x FD-CAN, 2x Gbit Ethernet with Time-Sensitive Networking (TSN) support, dual channel LVDS, HDMI, PCIe, 1x USB 3.0, 2x MIPI® CSI-2 for camera connection and many more.

The SoM is available with an optional dual-band Wi-Fi IEEE802.11 a/b/g/n/ac and Bluetooth 5.0 (BR / EDR / BLE) interface with chip antenna or U.FL connector.

Applications:

- Industrial Automation
- Machine controls and operator panels (HMI)
- Home & Building
- Medical Technology

1.2 Software

The DHCM-iMX8ML-01D2 uses Linux as operating system and the Board Support Package (BSP) comes with all necessary drivers and is Yocto Project based. With it, the customer has the opportunity to generate its own customer-specific operating system images suitable on our development kits.
The DHCM-iMX8ML-01D2 module is from the beginning on **up streamed** to **mainline U-Boot** and **Linux**.
Therefore, the user has the opportunity to switch very easy to the newest available Linux kernel release. The vendor-based support of DH electronics is in that case always based on latest LTS kernel version.

All available sources are available via Github: https://github.com/dh-electronics

Please also have a look at our Wiki: https://wiki.dh-electronics.com/index.php/DHCOM_iMX8-D2

1.3 Main features

- Quad ARM Cortex®-A53 up to 1.8 GHz and Single ARM Cortex®-M7 up to 800 MHz
- 3D GPU OpenGL® ES 3.0, OpenCL® 1.2, and Vulkan®.
- Power Management: Single SoM power supply with 3.3V or 5.0V
- Neuronal Processing Unit (NPU) with 2.3 TOPS to accelerate machine learning inferences
- LPDDR4: 1 / 2 / 4 Gbyte
- eMMC flash: 8 / 16 / 32 Gbyte
- SPI boot flash: 16 Mbyte
- EEPROM: 256 byte
- Wi-Fi® / Bluetooth: Wi-Fi® IEEE 802.11 a / b / g / n / ac with dual band, Bluetooth® v5.0 (BR/EDR/BLE), chip antenna or U.FL antenna connector
- On-board microSD card socket with support for SDR 104
- RTC with temperature compensation ± 3.0 ppm between -40 to +85°C
- Supply voltage range: 3.3 or 5.0 VDC / typ. 2.5 W-4 W (without Wi-Fi®/BT)
- Industrial temperature range: -40°C to +85°C
- SODIMM-200 socket with DHCOM pin assignment
- JTAG debug connection via FFC connector or Tag-Connect
- Gbit/s Ethernet or 100 Mbit/s Ethernet with support for Time Sensitive Networking (TSN)
- Ethernet 1: Gbit Ethernet or 100 Mbit Ethernet with PHY and support for Time Sensitive Networking
- Ethernet 2: 100 Mbit Ethernet with PHY or RGMII for Gbit Ethernet support
- MMC/SD interface: 4 bit mode
- CAN 1: V2.0B and CAN FD
- CAN 2: V2.0B and CAN FD
- UART 1: Rx / Tx / Rts / Cts, up to 4 Mbit/s
- UART 2: Rx / Tx / Rts / Cts, up to 4 Mbit/s
- UART 3: Rx / Tx, up to 4 Mbit/s
- SPI 1: max. 52 Mbit/s
- SPI 2: max. 52 Mbit/s
- I2C™ 1: max. 320 kbit/s
- I2C™ 2: max. 320 kbit/s
- USB host 1: High-Speed
- USB OTG: High-Speed

- Display RGB: Max. 1920 x 1080 pixels, 24 bit
- LVDS 4 data lanes or MIPI®-DSI 4 data lanes up to 1.5 Gbps
- Touch: 4-wire resistive
- I²S Audio interface
- GPIOs: 23 IOs
- PWM: 1x 16 bit
- Analog: 4x 12 bit ADC
- PCIe: 1-lane PCI Express Gen 3
- MIPI® CSI-2 1: 2-lanes up to 1.5 Gbps
- MIPI® CSI-2 2: 4-lanes up to 1.5 Gbps
- HDMI: 2.0a up to 1080p 60 fps
- USB 3.0: 2x

2 Hardware overview

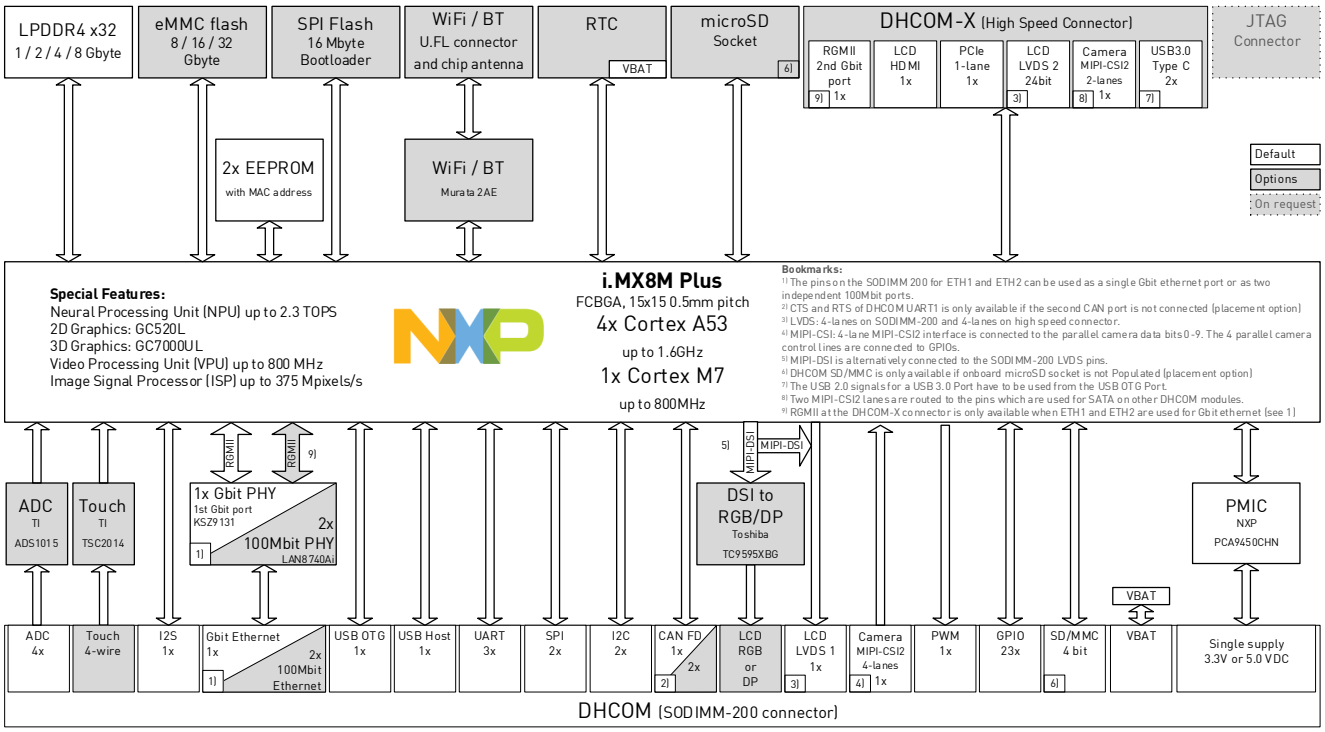

Figure 1: DHCM-iMX8ML-01D2 block diagram

2.1 Ordering options and configuration

For ordering information's and configuration options please have a look at the datasheet: https://www.dh-electronics.com/en/datasheet/dhcom-imx8m-plus

2.2 Connector overview

The DHCOM standard comes with two connectors.

- DHCOM SODIMM-200 = Main connector (always available)
- DHCOM-X high-speed connector = Connection to high-speed interfaces (optional available)

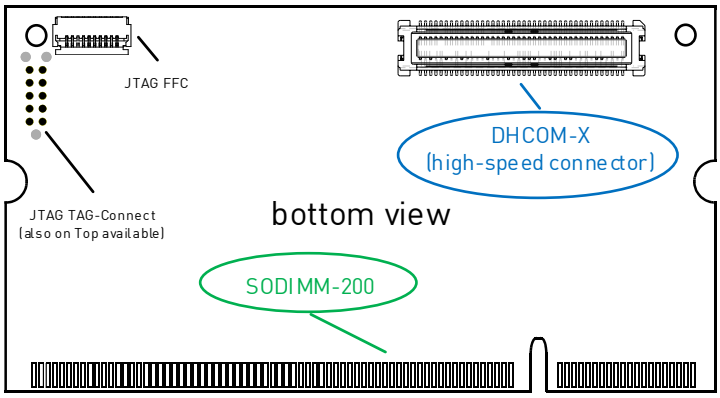

Figure 2: Connector description

The green marked table columns belong to **DHCOM SODIMM-200** connector and the blue marked to **DHCOM-X high-speed** connector.

2.3 Plugs and connections

2.3.1 DHCOM SODIMM-200

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
1	I2S_RXFS	VIO	2	Analog Input 3	Vref_ADC
3	Microphone GND (connected to GND)	VDDA	4	Analog Input 2	Vref_ADC
5	I2S_RXD	VIO	6	Analog Input 1	Vref_ADC
7	I2S_RXC	VIO	8	Analog Input 0	Vref_ADC
9	Audio GND (connected to GND)	VDDA	10	VDDA (not used)	VDDA
11	I2S_TXFS	VIO	12	TSPX	VIO
13	I2S_TXC	VIO	14	TSMX	VIO
15	I2S_TXD	VIO	16	TSMY	VIO
17	GND1	Vin	18	TSPY	VIO
19	GND2	Vin	20	RESET_OUT	VIO
21	RESET_IN	VIO	22	*Reserved*	VIO
23	UART3_RX	VIO	24	UART1_CTS or CAN2_TX	VIO
25	UART3_TX	VIO	26	UART1_RTS or CAN2_RX	VIO
27	CAN_TX	VIO	28	*Reserved*	VIO
29	CAN_RX	VIO	30	*Reserved*	VIO
31	UART2_CTS	VIO	32	UART1_RX	VIO
33	UART2_RTS	VIO	34	UART1_TX	VIO
35	UART2_RX	VIO	36	*Reserved*	VIO
37	UART2_TX	VIO	38	VCC_IN1	Vin
39	VCC_IN2	Vin	40	VCC_IN3	Vin
41	VCC_IN4	Vin	42	VCC_IN5	Vin
43	GND3	Vin	44	VCC_IN6	Vin
45	GND4	Vin	46	Vdisp_OUT	Vdisp or CSI
47	GND5	Vin	48	GPIO_W or CSI2_CLK+	Vcam or CSI
49	LC_R2 or DPLNM0	Vdisp or DP	50	GPIO_V or CSI2_CLK-	Vcam or CSI
51	LC_R3 or DPLNP0	Vdisp or DP	52	GPIO_U or CSI2_D0+	Vcam or CSI
53	LC_R4 or DPLNM1	Vdisp or DP	54	GPIO_T or CSI2_D0-	Vcam or CSI
55	LC_R5 or DPLNP1	Vdisp or DP	56	GPIO_S or CSI2_D1+	Vcam or CSI
57	LC_R6 or DPAUXM	Vdisp or DP	58	GPIO_R or CSI2_D1-	Vcam or CSI
59	LC_R7 or DPAUXP	Vdisp or DP	60	GPIO_Q or CSI2_D2+	Vcam or CSI
61	LC_G2 or DP HPD	Vdisp	62	GPIO_P or CSI2_D2-	Vcam or CSI
63	LC_G3	Vdisp	64	GPIO_O or CSI2_D3+	Vcam or CSI
65	LC_G4	Vdisp	66	GPIO_N or CSI2_D3-	Vcam or CSI
67	LC_G5	Vdisp	68	GPIO_M or CSIx_MCLK	Vcam or CSI
69	LC_G6	Vdisp	70	GPIO_L or CSI2_SYNC	Vcam
71	LC_G7	Vdisp	72	GPIO_K or CSIx_PWDN	Vcam
73	LC_B2	Vdisp	74	GPIO_J or CSIx_#RST	Vcam

Pin number	Pin name	Power domain
75	LC_B3	Vdisp
77	LC_B4	Vdisp
79	LC_B5	Vdisp
81	LC_B6	Vdisp
83	LC_B7	Vdisp
85	LC_EN	Vdisp
87	LC_VSYNC	Vdisp
89	LC_HSYNC	Vdisp
91	LC_PCLK	Vdisp
93	LVDS_TX2+ or DSI_D2_P	LVDS or DSI
95	LVDS_TX2- or DSI_D2_N	LVDS or DSI
97	LVDS_CLK+ or DSI_CK_P	LVDS or DSI
99	LVDS_CLK- or DSI_CK_N	LVDS or DSI
101	GND6	Vin
103	SD_CLK	VIO
105	SD_DETECT	VIO
107	SD_D1	VIO
109	SD_D3	VIO
111	GND7	Vin
113	*Reserved*	Vsysbus
115	*Reserved*	Vsysbus
117	*Reserved*	Vsysbus
119	*Reserved*	Vsysbus
121	*Reserved*	Vsysbus
123	*Reserved*	Vsysbus
125	*Reserved*	Vsysbus
127	*Reserved*	Vsysbus
129	*Reserved*	Vsysbus
131	*Reserved*	Vsysbus
133	*Reserved*	Vsysbus
135	*Reserved*	Vsysbus
137	*Reserved*	Vsysbus
139	*Reserved*	Vsysbus
141	*Reserved*	Vsysbus
143	*Reserved*	Vsysbus
145	*Reserved*	Vsysbus
147	*Reserved*	Vsysbus
149	*Reserved*	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO
153	GND8	Vin
155	SPI2_CS0	VIO
157	SPI2_CLK	VIO
159	SPI2_MISO	VIO
161	SPI2_MOSI	VIO
163	GPIO_D	VIO
165	GPIO_F	VIO
167	GPIO_G	VIO

Pin number	Pin name	Power domain
76	LC_R0	Vdisp
78	LC_R1	Vdisp
80	LC_G0	Vdisp
82	LC_G1	Vdisp
84	LC_B0	Vdisp
86	LC_B1	Vdisp
88	LVDS_TX0+ or DSI_D0_P	LVDS or DSI
90	LVDS_TX0- or DSI_D0_N	LVDS or DSI
92	LVDS_TX1+ or DSI_D1_P	LVDS or DSI
94	LVDS_TX1- or DSI_D1_N	LVDS or DSI
96	LVDS_TX3+ or DSI_D3_P	LVDS or DSI
98	LVDS_TX3- or DSI_D3_N	LVDS or DSI
100	GPIO_PWM	VIO
102	Vcam_OUT	Vcam
104	SD_CMD	VIO
106	SD_D0	VIO
108	SD_D2	VIO
110	Vsysbus_OUT	Vsysbus
112	*Reserved*	Vsysbus
114	*Reserved*	Vsysbus
116	*Reserved*	Vsysbus
118	*Reserved*	Vsysbus
120	*Reserved*	Vsysbus
122	*Reserved*	Vsysbus
124	*Reserved*	Vsysbus
126	*Reserved*	Vsysbus
128	*Reserved*	Vsysbus
130	*Reserved*	Vsysbus
132	*Reserved*	Vsysbus
134	*Reserved*	Vsysbus
136	*Reserved*	Vsysbus
138	*Reserved*	Vsysbus
140	*Reserved*	Vsysbus
142	*Reserved*	Vsysbus
144	*Reserved*	Vsysbus
146	*Reserved*	Vsysbus
148	*Reserved*	Vsysbus
150	*Reserved*	Vsysbus
152	VIO_OUT	VIO
154	GPIO_A	VIO
156	GPIO_B	VIO
158	I2C2_CLK	VIO
160	I2C2_DATA	VIO
162	GPIO_C	VIO
164	GPIO_E	VIO
166	USB_OTG_VBUS	USB
168	USB_OTG_ID	VIO

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
169	*Reserved*	USB	170	USB_OTG_D+	USB
171	*Reserved*	USB	172	USB_OTG_D-	USB
173	GPIO_H	VIO	174	USB_PWR_STAT	VIO
175	GPIO_I	VIO	176	USB_PWR_EN	VIO
177	SPI1_CS0	VIO	178	USB_HOST_D1+	USB
179	SPI1_CLK	VIO	180	USB_HOST_D1-	USB
181	SPI1_MISO	VIO	182	I2C1_CLK	VIO
183	SPI1_MOSI	VIO	184	I2C1_DATA	VIO
185	GND9	Vin	186	nETH1_LINK_LED or LED2	VIO or OC
187	nETH2_LINK_LED	VIO	188	nETH1_SPEED_LED or LED1	VIO or OC
189	nETH2_SPEED_LED	VIO	190	ETH1_TXD- or TXRX_A-	Ethernet
191	ETH2_TXI- or TXRX_C-	Ethernet	192	ETH1_TXD+ or TXRX_A+	Ethernet
193	ETH2_TXI+ or TXRX_C+	Ethernet	194	ETH_VIO_SWITCHED	VIO
195	ETH2_RXI- or TXRX_D-	Ethernet	196	ETH1_RXI- or TXRX_B-	Ethernet
197	ETH2_RXI+ or TXRX_D+	Ethernet	198	ETH1_RXI+ or TXRX_B+	Ethernet
199	GND10	Vin	200	VCC_BAT	Vbat

Table 1: SODIMM-200 pin assignment

2.3.2 DHCOM-X high-speed

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
1	RGMII_RXCLK	Vrgmii	2	RGMII_TXCLK	Vrgmii
3	RGMII_RXD0	Vrgmii	4	RGMII_TXD0	Vrgmii
5	RGMII_RXD1	Vrgmii	6	RGMII_TXD1	Vrgmii
7	RGMII_RXD2	Vrgmii	8	RGMII_TXD2	Vrgmii
9	RGMII_RXD3	Vrgmii	10	RGMII_TXD3	Vrgmii
11	RGMII_RX_CTL	Vrgmii	12	RGMII_TX_CTL	Vrgmii
13	RGMII_MDIO	Vrgmii	14	RGMII_MDC	Vrgmii
15	RGMII_RST	Vrgmii	16	RGMII_REFCLK	Vrgmii
17	RGMII_WOL_INT	3V3	18	RGMII_INT	3V3
19	GND	Vin	20	VCC_RGMII_OUT	Vrgmii
21	*CSI_D2+ (on request)*	CSI	22	GND	Vin
23	*CSI_D2- (on request)*	CSI	24	*CSI_D3+ (on request)*	CSI
25	GND	Vin	26	*CSI_D3- (on request)*	CSI
27	PCIE_RX+	PCIe	28	GND	Vin
29	PCIE_RX-	PCIe	30	PCIE_REFCLK+	PCIe
31	PCIE_TX+	PCIe	32	PCIE_REFCLK-	PCIe
33	PCIE_TX-	PCIe	34	PCIE_WAKE	3V3
35	GND	Vin	36	GND	Vin
37	CSI_CLK+	CSI	38	CSI_D0+	CSI
39	CSI_CLK-	CSI	40	CSI_D0-	CSI
41	GND	Vin	42	CSI_D1+	CSI
43	HDMI_CLK+	HDMI	44	CSI_D1-	CSI
45	HDMI_CLK-	HDMI	46	GND	Vin
47	HDMI_D2+	HDMI	48	HDMI_D0+	HDMI
49	HDMI_D2-	HDMI	50	HDMI_D0-	HDMI

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
51	HDMI_CEC	3V3	52	HDMI_D1+	HDMI
53	GND	Vin	54	HDMI_D1-	HDMI
55	LVDS2_CLK+	LVDS	56	HDMI_HPD	3V3
57	LVDS2_CLK-	LVDS	58	GND	Vin
59	LVDS2_TX2+	LVDS	60	LVDS2_TX0+	LVDS
61	LVDS2_TX2-	LVDS	62	LVDS2_TX0-	LVDS
63	LVDS2_TX3+	LVDS	64	LVDS2_TX1+	LVDS
65	LVDS2_TX3-	LVDS	66	LVDS2_TX1-	LVDS
67	GND	Vin	68	GND	Vin
69	USB_SS_TX1+	USB	70	USB_SS_TX2+	USB
71	USB_SS_TX1-	USB	72	USB_SS_TX2-	USB
73	USB_SS_RX1+	USB	74	USB_SS_RX2+	USB
75	USB_SS_RX1-	USB	76	USB_SS_RX2-	USB
77	USB_SS_INT	3V3	78	*Reserved*	-
79	VCC_IN7	Vin	80	VCC_IN8	Vin

Table 2: DHCOM-X connector pin assignment

2.3.3 JTAG

The DHCOM i.MX8M Plus module offers two different JTAG connections. The interface usually is not required for programming the SoM. However, it can be helpful for debugging the Cortex-M7 Core or very advanced debugging of the Cortex-A Cores.

2.3.3.1 FFC connector

Pin number	Pin name (JTAG-Mode)
1	+3V3 Output
2	GND
3	JTAG_TMS
4	-
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	*Reserved*
10	*Reserved*

Table 3: FFC JTAG interface pin assignment

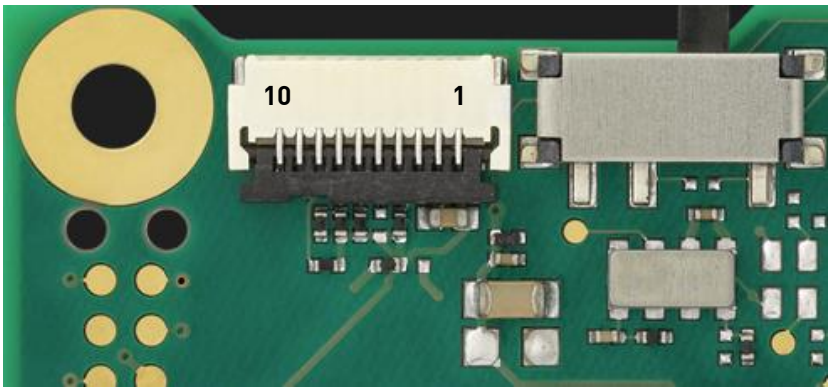

Figure 3: Pin assignment of the FFC JTAG connector which has top and bottom contacts (Wuerth Elektronik: 687110182122)

2.3.3.2 TAG-Connect

Pin number	Pin name (JTAG-Mode)
1	+3V3 Output
2	JTAG_TMS
3	GND
4	JTAG_TCK
5	*Reserved*
6	JTAG_TDO
7	*Reserved*
8	JTAG_TDI
9	*Reserved*
10	#RESET_IN

Table 4: Tag-Connect JTAG interface pin assignment

Figure 4: TAG Connect pin assignment on the topside of the DHCOM i.MX8M Plus to use with a TC2050-IDC-NL cable

3 DHCOM Standard and compatibility

Please have a look at the DHCOM standard specification: https://wiki.dh-electronics.com/images/2/2e/DOC_DHCOM-Standard-Specification_R01_2016-11-17.pdf

4 Power supply and reset

4.1.1 Power supply

The DHCOM i.MX8M Plus has the following power connections:

- Vin = Core module supply voltage input
- V_{BAT} = Battery voltage input
- V_{SYSBUS} = System bus reference voltage output
- V_{DISP} = Display reference voltage output
- V_{CAM} = Camera reference voltage output
- V_{IO} = I/O reference voltage output
- $V_{CC\_RGMII\_OUT}$ = RGMII reference voltage output

The following table shows an overview about the DHCOM voltage groups and the differences between the available System on Modules.

Voltage	i.MX6UL(L)	AM335x	STM32MP1	i.MX6	i.MX8M Plus
VCC (Vin)	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V
V_{BAT}	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V	1.2V – **5.5V**
V_{SYSBUS}	Not available (3.3V)	Not available (3.3V)	3.3V	3.3V	Not available (3.3V)
V_{DISP}	3.3V	3.3V	3.3V	3.3V	**1.8V**
V_{CAM}	3.3V	3.3V	3.3V	3.3V	3.3V
V_{IO}	3.3V	3.3V	3.3V	3.3V	3.3V
$V_{ETH\_VIO\_SWITCHED}$	3.3V	3.3V	3.3V	3.3V	3.3V
USB_OTG_VBUS	5.0V	5.0V	5.0V	5.0V	5.0V
$V_{CC\_RGMII\_OUT}$	Not available	Not available	3.3V	2.5V	1.8V

Table 5: Voltage groups

Notes to V_{BAT}:

- When no buffer battery is used in the system, V_{BAT} must be connected to 3.3V.
- In applications, where date and time buffering are needed, we recommend the option [-RTC] (for more details have a look at 2.1 Ordering options and configuration), which uses the RV-3032-C7 instead of the internal RTC. This external RTC supports temperature compensation which leads to a higher accuracy and is running with a very low power consumption. When ordering the DHCOM i.MX8M Plus with the option [-RTC], V_{BAT} is connected to the RV-3032-C7. For more information about this option have a look at chapter 8.5 “RTC”.

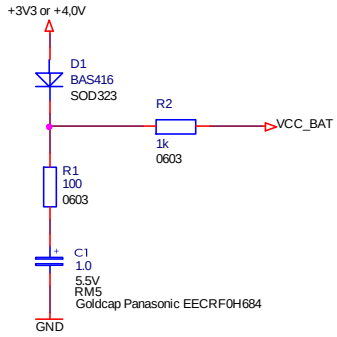

Figure 5: Vbat GoldCap example

The power supply connections Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT are to be used to detect the correct voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with the level shifter.

4.1.2 Reset signals

The System is put in reset state by holding RESET_IN signal low.

When the RESET_IN is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_OUT is asserted as long as RESET_IN is asserted. If the reset input RESET_IN is de-asserted, the RESET_OUT is also de-asserted and the module starts booting again.

4.1.3 Supply Overview

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
VCC_IN1	Core Module supply voltage input	38	PWR_I	-	MBC
VCC_IN2	Core Module supply voltage input	39	PWR_I	-	MBC
VCC_IN3	Core Module supply voltage input	40	PWR_I	-	MBC
VCC_IN4	Core Module supply voltage input	41	PWR_I	-	MBC
VCC_IN5	Core Module supply voltage input	42	PWR_I	-	MBC
VCC_IN6	Core Module supply voltage input	44	PWR_I	-	MBC
GND1	Core Module Ground	17	PWR_I	-	MBC
GND2	Core Module Ground	19	PWR_I	-	MBC
GND3	Core Module Ground	43	PWR_I	-	MBC
GND4	Core Module Ground	45	PWR_I	-	MBC
GND5	Core Module Ground	47	PWR_I	-	MBC
GND6	Core Module Ground	101	PWR_I	-	MBC
GND7	Core Module Ground	111	PWR_I	-	MBC
GND8	Core Module Ground	153	PWR_I	-	MBC
GND9	Core Module Ground	185	PWR_I	-	MBC
GND10	Core Module Ground	199	PWR_I	-	MBC
VCC_BAT	Core Module Battery voltage input	200	PWR_I	-	MBC
VDDA_Audio	Audio Codec supply voltage input (Not connected on the DHCOM i.MX8M Plus, because the module is not available with onboard Audio Codec)	10	PWR_I	-	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	-	MBC

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
Vcam_OUT	Camera supply voltage output	102	PWR_O	-	-
VIO_OUT	I/O supply voltage output	152	PWR_O	-	-
RESET_IN	System Reset input (active low)	21	I	-	-
RESET_OUT	System Reset output (active low)	20	O	-	-

Table 6: SODIMM-200 Power supply and reset

Notes:

- On the DHCOM i.MX8M Plus VDDA_Audio is not used; it also can be left unconnected. However, in order to support all our DHCOM modules, it is recommended to connect it. Please connect it to V_{IO_OUT}. (See 3 DHCOM Standard and compatibility)

DHCOM-X pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
VCC_IN7	Core Module supply voltage input	79	PWR_I	-	SBC
VCC_IN8	Core Module supply voltage input	80	PWR_I	-	SBC
GND11	Core Module Ground	19	PWR_I		SBC
GND12	Core Module Ground	22	PWR_I		SBC
GND13	Core Module Ground	25	PWR_I		SBC
GND14	Core Module Ground	28	PWR_I		SBC
GND15	Core Module Ground	35	PWR_I	-	SBC
GND16	Core Module Ground	36	PWR_I	-	SBC
GND17	Core Module Ground	41	PWR_I	-	SBC
GND18	Core Module Ground	46	PWR_I	-	SBC
GND19	Core Module Ground	53	PWR_I	-	SBC
GND20	Core Module Ground	58	PWR_I	-	SBC
GND21	Core Module Ground	67	PWR_I	-	SBC
GND22	Core Module Ground	68	PWR_I	-	SBC
VCC_RGMII_OUT	1,8V Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	-	-

Table 7: DHCOM-X Power supply

5 Hardware coding

The following pins can be used to identify the current hardware version of the DHCOM i.MX8M Plus module.

CPU ball name	Description	IO Type
NAND_DQS	Code_HW_0	I
SAI1_TXD7	Code_HW_1	I
SAI5_MCLK	Code_HW_2	I

Table 8: Hardware coding

DH PCB number	Description	Code_HW_2	Code_HW_1	Code_HW_0
660-100 (prototype)	DHCM-iMX8ML-01D2 HW100	0 (10k PD)	0 (10k PD)	0 (10k PD)
660-200 (current version)	DHCM-iMX8ML-01D2 HW200	0 (10k PD)	0 (10k PD)	1 (10k PU)
...		0 (10k PD)	1 (10k PU)	0 (10k PD)
		0 (10k PD)	1 (10k PU)	1 (10k PU)
		1 (10k PU)	0 (10k PD)	0 (10k PD)

Table 9: PCB versions

6 Boot Mode

During startup the DHCOM i.MX8M Plus reads out the BOOT-Pins to select a specific boot mode.

BOOT3	BOOT2	BOOT1	BOOT0	Initial boot mode	Comment
0	0	0	0	Boot from internal fuses	
0	0	0	1	USB serial download	-> For development usage or commissioning
0	0	1	0	USDHC3 (eMMC)	-> OnBoard eMMC
0	0	1	1	USDHC2 (SD)	-> OnBoard microSD
~~0~~	~~1~~	~~0~~	~~0~~	~~NAND 8-bit device, 256 pages~~	*Not available*
~~0~~	~~1~~	~~0~~	~~1~~	~~NAND 8-bit device, 512 pages~~	*Not available*
0	**1**	**1**	**0**	**FlexSPI 3B Read**	-> OnBoard SPI Flash = **DEFAULT boot mode**
~~0~~	~~1~~	~~1~~	~~1~~	~~FlexSPI Hyperflash 3.3V~~	*Not available*
~~1~~	~~0~~	~~0~~	~~0~~	~~eCSPI Boot~~	*Not available*
~~1~~	~~0~~	~~0~~	~~1~~	~~Reserved~~	*Not available*
~~1~~	~~0~~	~~1~~	~~0~~	~~FLEXSPI serial NAND, 2k page~~	*Not available*
~~1~~	~~0~~	~~1~~	~~1~~	~~FLEXSPI serial NAND, 4k page~~	*Not available*

Table 10: Combination of the BOOT-Pins to select a boot mode

As a default, the boot mode is set to Serial NOR Flash, to start up from the on-board SPI boot flash, which contains a **factory preprogrammed bootloader**. The bootloader can afterwards start the operating system from other flash devices like eMMC or SD card.

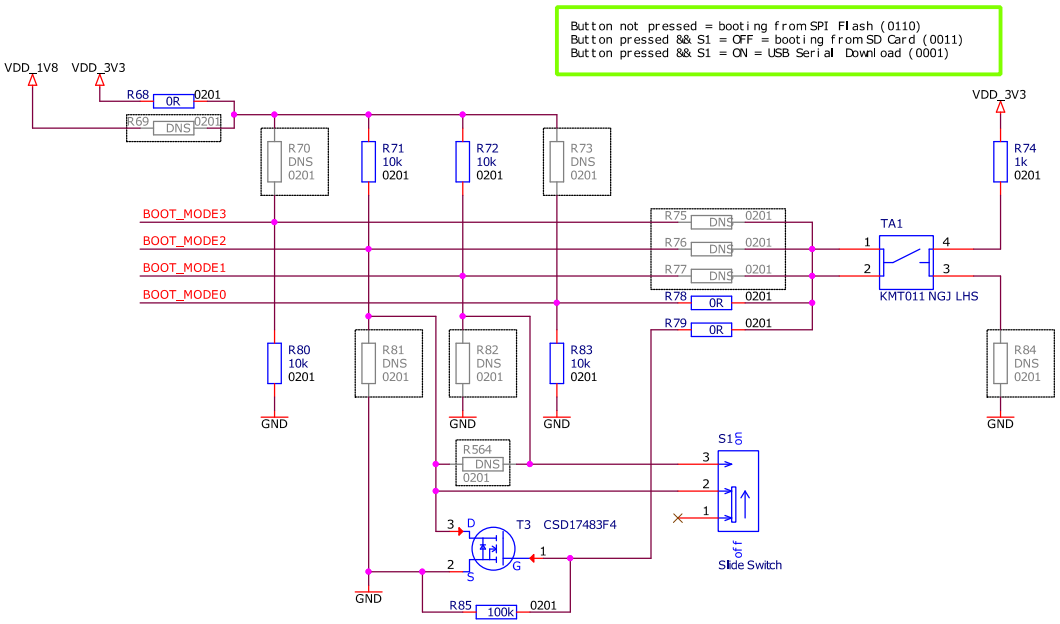

Figure 6: Selection of the boot mods with push-button to switch to a different mode temporarily

In Addition to that, the DHCOM i.MX8M Plus contains a push-button and switch which can be used to override the boot-pins temporarily. For instance, if switch S1 is in OFF mode, the boot-mode can be switched from Serial NOR Flash to SD card by holding down the button during the first seconds of boot-up. And if switch S1 is in ON mode, pressing the button results in USB serial downloader mode.

However, this button is meant for development use only and therefore it is not populated when it comes to the mass production.

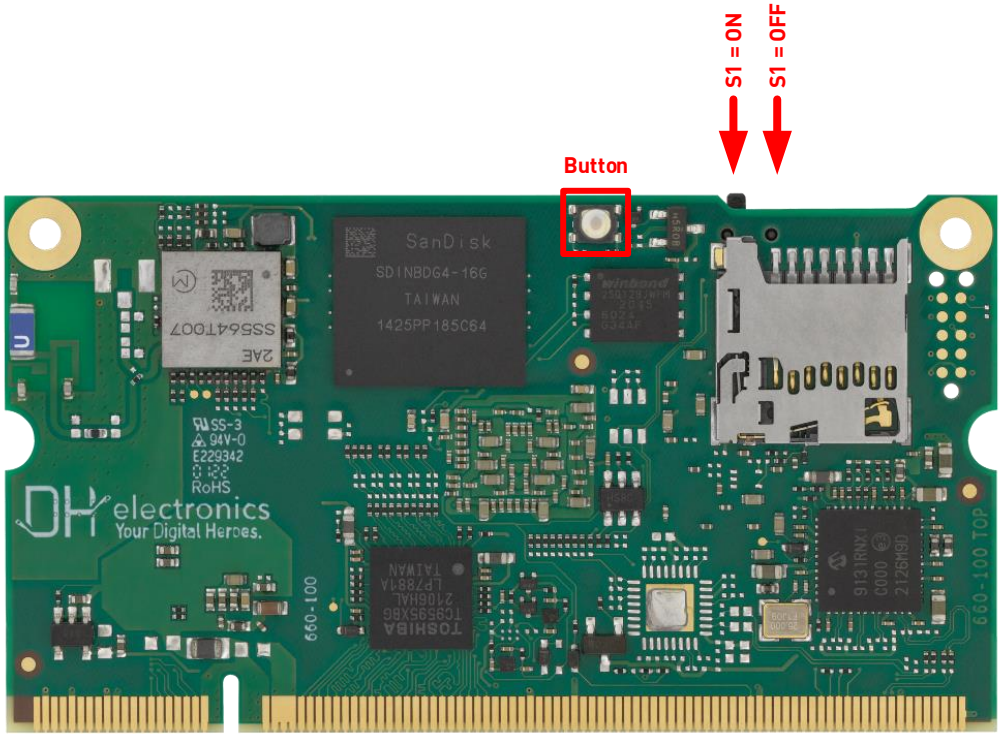

Figure 7: BOOT configuration on the topside of the DHCOM i.MX8M Plus

7 Interface description

The following subsections describe the signals at the DHCOM SODIMM-200 socket and the DHCOM-X high-speed connector.

Notes:

- For all specified pull-up and pull-down resistors, a value of 10k is recommended.
- "Not used" specification describes, what needs to be done with unconnected pins.

7.1 Ethernet

The DHCOM i.MX8M Plus provides different Ethernet options:

1. 2x 1Gbit/s Ethernet interfaces: First port with PHY on module and second port via RGMII.

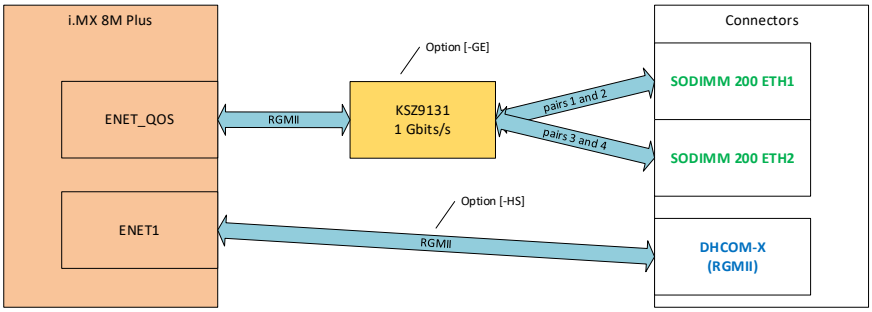

Figure 8: 2x 1Gbit/s Ethernet

2. 2x 100Mbit/s Ethernet interfaces: Both ports with PHY on module.

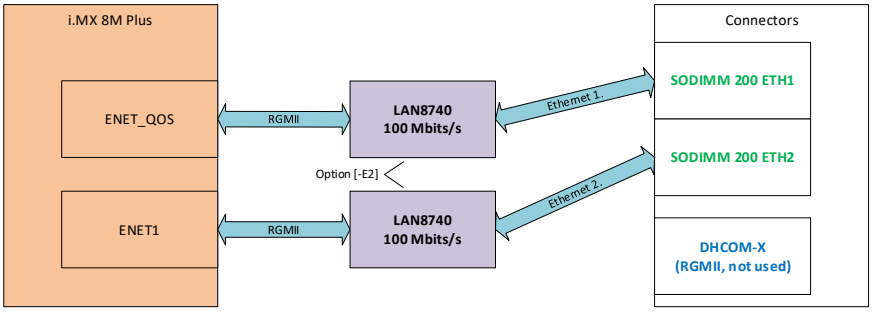

Figure 9: 2x 100Mbit/s Ethernet

3. 1x 100Mbit/s + 1x 1Gbit/s Ethernet interfaces: 100Mbit/s PHY on module and second port via RGMII.

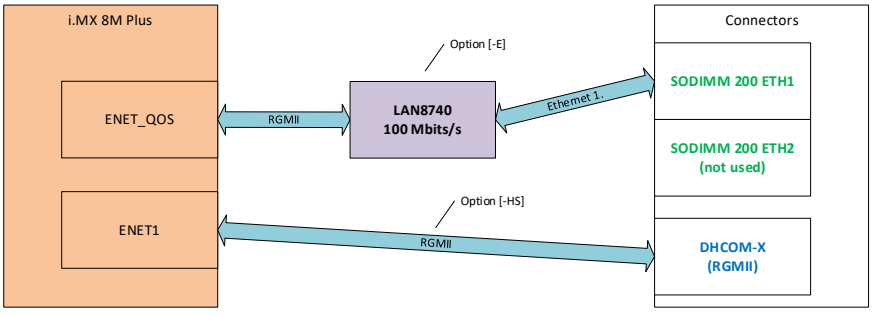

Figure 10: 1x 1Gbit/s + 1x 100Mbit/s Ethernet

Notes:

- Ordering information:
  - Option 1 with RGMII available at DHCOM-X connector: DHCM-iMX8ML...-**GE**...-**HS**...
  - Option 1 without RGMII available at DHCOM-X connector: DHCM-iMX8ML...-**GE**...
  - Option 2: DHCM-iMX8ML...-**E2**...
  - Option 3 with RGMII available at DHCOM-X connector: DHCM-iMX8ML...-**E**...-**HS**...
  - Option 3 without RGMII available at DHCOM-X connector: DHCM-iMX8ML...-**E**...

  See also 2.1 Ordering options and configuration.

7.1.1 2x 1Gbit/s Ethernet

The DHCOM i.MX8M Plus offers two 1Gbit/s Ethernet interfaces. First port with PHY on module and second port via RGMII.

7.1.1.1 ETH1 with PHY on SODIMM-200

The Ethernet ENET_QOS interface of the i.MX8M Plus is connected via RGMII mode to the PHY KSZ9131 from Microchip.

The i.MX8M Plus is also connected via I2C™ to a separate EEPROM which contains a MAC address for the ETH1 interface. The I2C™ address of the EEPROM is 0x50. (See also 7.9.3 On-module I2CTM)

The Ethernet interface fulfil the IEEE1588 conform standard.

The ENET_QOS supports the following Time Sensitive Networking (TSN) features:

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qbu Frame preemption
- Time based Scheduling

Notes:

- The KSZ9131 design incorporates voltage-mode transmit drivers and on-chip terminations.

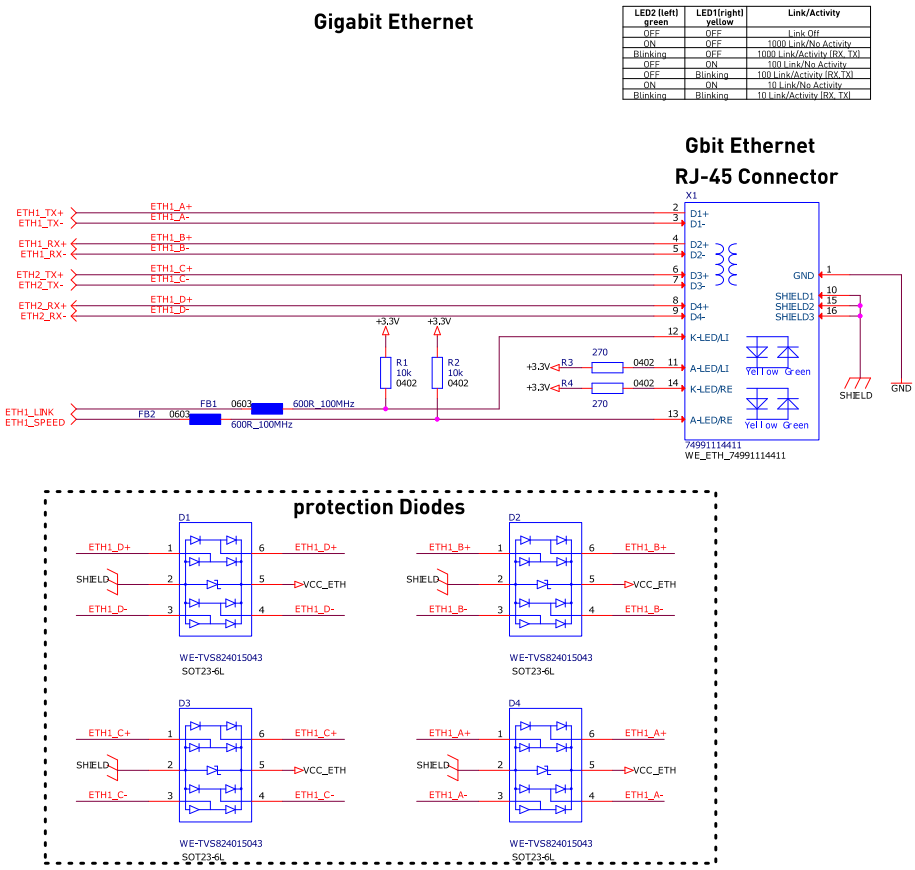

Figure 11: 1Gbit/s example

- LED description:
  - nETH1_LINK_LED = Gbit/s port: LED2
  - nETH1_SPEED_LED = Gbit/s port: LED1

LED2	LED1	Link/Activity
OFF	OFF	Link off
ON	OFF	1000 link/no activity
Blinking	OFF	1000 link/activity (Rx, Tx)
OFF	ON	100 Link/no activity
OFF	Blinking	100 link/activity (Rx, Tx)
ON	ON	10 Link/no activity
Blinking	Blinking	10 link/activity (Rx, Tx)

Table 11: 1Gbit/s Ethernet LED description

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
nETH1_LINK_LED	Gbit/s port: LED2	186	O	-	PU
nETH1_SPEED_LED	Gbit/s port: LED1	188	O	-	PU
ETH1_TXD-	Gbit/s port: Ethernet TXRX_A-	190	IO	-	PD
ETH1_TXD+	Gbit/s port: Ethernet TXRX_A+	192	IO	-	PD
~~ETH_VIO_SWITCHED~~	*Not used*	194	PWR_O	-	-
ETH1_RXI-	Gbit/s port: Ethernet TXRX_B-	196	IO	-	PD
ETH1_RXI+	Gbit/s port: Ethernet TXRX_B+	198	IO	-	PD

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
~~nETH2_LINK_LED~~	*Not used*	187	O	-	-
~~nETH2_SPEED_LED~~	*Not used*	189	O	-	-
ETH2_TXD-	Gbit/s port: Ethernet TXRX_C-	191	IO	-	PD
ETH2_TXD+	Gbit/s port: Ethernet TXRX_C+	193	IO	-	PD
ETH2_RXI-	Gbit/s port: Ethernet TXRX_D-	195	IO	-	PD
ETH2_RXI+	Gbit/s port: Ethernet TXRX_D+	197	IO	-	PD

Table 12: Gbit/s Ethernet connection

7.1.1.2 ETH2 via RGMII on DHCOM-X

Like mentioned in the beginning of this chapter, the RGMII interface is only available when ordering an DHCOM i.MX8M Plus with the option [-HS]. Next to this it is necessary, that the RGMII port is not used for the second 100Mbit/s PHY. Please have a look at 7.1 Ethernet, there you find a detailed description of the available options. The RGMII interface is available on the additional DHCOM-X connector of the DHCOM module.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
RGMII_RXCLK	Receive Reference Clock	1	I	SAI1_TXC	-
RGMII_RXD0	Receive Data 0	3	I	SAI1_RXD4	-
RGMII_RXD1	Receive Data 1	5	I	SAI1_RXD5	-
RGMII_RXD2	Receive Data 2	7	I	SAI1_RXD6	-
RGMII_RXD3	Receive Data 3	9	I	SAI1_RXD7	-
RGMII_RX_CTL	Receive Control	11	O	SAI1_TXFS	-
RGMII_MDIO	Management Data Input / Output	13	IO	SAI1_RXD3	-
RGMII_RST	Ethernet Reset	15	O	SAI1_RXD0	-
RGMII_WOL_INT	Wake on LAN interrupt (3V3 capable)	17	I	SAI1_TXD6	-
RGMII_TXCLK	Transmit Reference Clock	2	O	SAI1_TXD5	-
RGMII_TXD0	Transmit Data 0	4	O	SAI1_TXD0	-
RGMII_TXD1	Transmit Data 1	6	O	SAI1_TXD1	-
RGMII_TXD2	Transmit Data 2	8	O	SAI1_TXD2	-
RGMII_TXD3	Transmit Data 3	10	O	SAI1_TXD3	-
RGMII_TX_CTL	Transmit Control	12	O	SAI1_TXD4	-
RGMII_MDC	Management Data Clock	14	O	SAI1_RXD2	-
RGMII_REFCLK	Not used with i.MX8M Plus (125 MHz Clock)	16	I	-	PU
RGMII_INT	Interrupt (3V3 capable)	18	I	SAI1_RXD1	PU
VCC_RGMII_OUT	Power Supply (1V8)	20	PWR_O	-	-

Table 13: RGMII Interface Connection

7.1.2 2x 100Mbit/s Ethernet

The DHCOM i.MX8M Plus provides two Ethernet interfaces with onboard PHY LAN8740 and up to 100BASE-TX full duplex.

Notes:

- The LED outputs “nETH*_LINK_LED” and “nETH*_SPEED_LED” must be connected as follows:

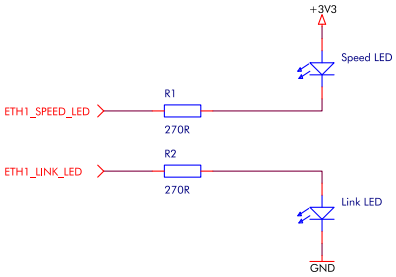

Table 14: Ethernet LED circuitry

- In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration straps.
- A special feature of the DHCOM Ethernet interface is the voltage output ETH_VIO_SWITCHED. This output can be used to supply the Ethernet transmitter. In case of low power modes, the output is disabled from the software to save power. The output is activated or deactivated via the IO Expander: I2C: 0x74; P0.2 (See also 7.9.3 On-module I2CTM)

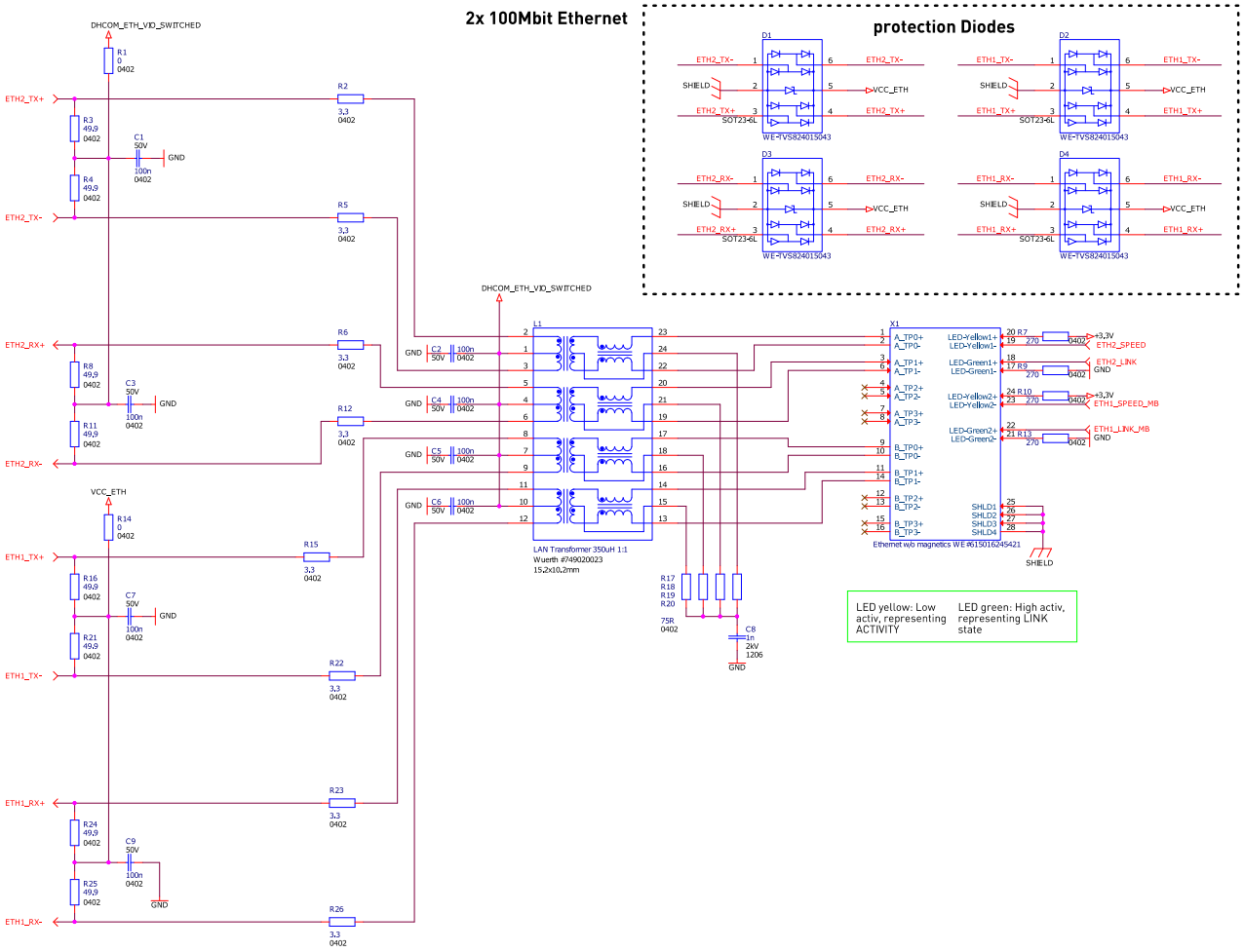

Figure 12: 2x 100Mbit/s example with ETH_VIO_SWITCHED

7.1.2.1 ETH1 with PHY on SODIMM-200

The Ethernet ENET_QOS interface of the i.MX8M Plus is connected via RMII mode to the PHY LAN8740Ai from Microchip.

The i.MX8M Plus is also connected via I2C™ to a separate EEPROM which contains a MAC address for the ETH1 interface. The I2C™ address of the EEPROM is 0x50. (See also 7.9.3 On-module I2CTM)

The Ethernet interface fulfil the IEEE1588 conform standard.

The ENET_QOS supports the following Time Sensitive Networking (TSN) features:

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qbu Frame preemption
- Time based Scheduling

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	-	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	-	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	-	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	-	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	- (I2C: 0x74; P0.2)	-
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	-	PD
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	-	PD

Table 15: Ethernet 1 Connection

7.1.2.2 ETH2 with PHY on SODIMM-200

The Ethernet ENET1 interface of the i.MX8M Plus is connected via RMII mode to a second PHY LAN8740Ai from Microchip.

The i.MX8M Plus is also connected via I2C™ to an additional EEPROM which contains a MAC address for the ETH2 interface. The I2CTM address of the EEPROM is 0x53. (See also 7.9.3 On-module I2CTM)

The Ethernet interface fulfil the IEEE1588 conform standard.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
nETH2_LINK_LED	Port 2: Activity LED connection	187	O	-	PD
nETH2_SPEED_LED	Port 2: Speed LED connection	189	O	-	PU
ETH2_TXD-	Port 2: Ethernet TX Differential Output (minus)	191	O	-	PD
ETH2_TXD+	Port 2: Ethernet TX Differential Output (plus)	193	O	-	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	- (I2C: 0x74; P0.2)	-
ETH2_RXI-	Port 2: Ethernet TX Differential Input (minus)	195	I	-	PD
ETH2_RXI+	Port 2: Ethernet TX Differential Input (plus)	197	I	-	PD

Table 16: Ethernet 2 Connection

7.1.3 1x 100Mbit/s + 1x 1Gbit/s Ethernet

The DHCOM i.MX8M Plus interfaces can be shared into one 100Mbit/s Ethernet with PHY onboard and a second interface (100Mbit/s or 1Gbit/s) connected via RGMII.

Notes:

- The LED outputs “nETH*_LINK_LED” and “nETH*_SPEED_LED” must be connected as follows:

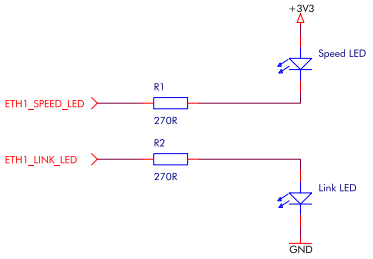

Table 17: Ethernet LED circuitry

- In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration straps.
- A special feature of the DHCOM Ethernet interface is the voltage output ETH_VIO_SWITCHED. This output can be used to supply the Ethernet transmitter. In case of low power modes, the output is disabled from the software to save power. The output is activated or deactivated via the IO Expander: I2C: 0x74; P0.2 (See also 7.9.3 On-module I2CTM)

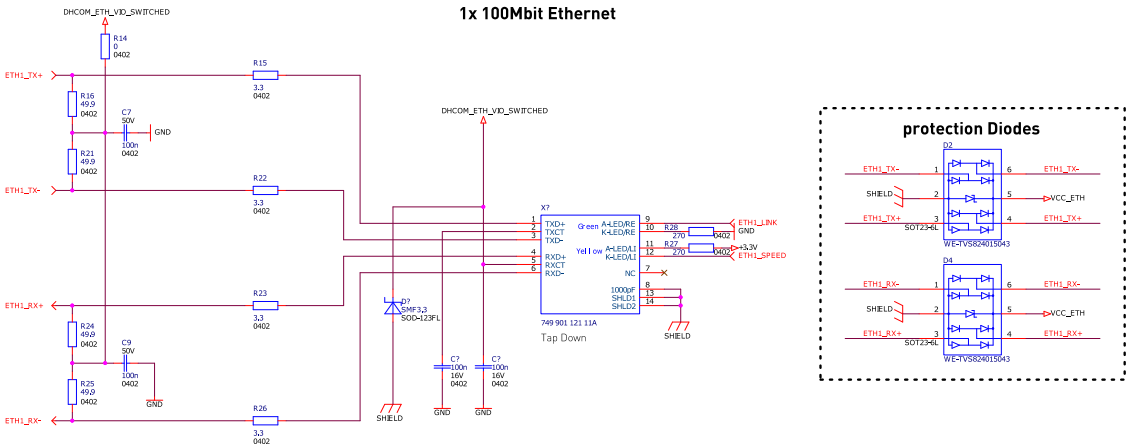

Figure 13: 1x 100Mbit/s example with ETH_VIO_SWITCHED

7.1.3.1 ETH1 with PHY on SODIMM-200

The Ethernet ENET_QOS interface of the i.MX8M Plus is connected via RMII mode to the PHY LAN8740Ai from Microchip.

The i.MX8M Plus is also connected via I2C™ to a separate EEPROM which contains a MAC address for the ETH1 interface. The I2C™ address of the EEPROM is 0x50. (See also 7.9.3 On-module I2CTM)

The Ethernet interface fulfil the IEEE1588 conform standard.

The ENET_QOS supports the following Time Sensitive Networking (TSN) features:

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qbu Frame preemption
- Time based Scheduling

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	-	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	-	PU

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	-	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	-	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	- (I2C: 0x74; P0.2)	-
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	-	PD
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	-	PD

Table 18: Ethernet 1 Connection

7.1.3.2 ETH2 via RGMII on DHCOM-X

Like mentioned in the beginning of this chapter, the RGMII interface is only available when ordering an DHCOM i.MX8M Plus with the option [-HS]. Next to this it is necessary, that the RGMII port is not used for the second 100Mbit/s PHY. Please have a look at 7.1 Ethernet, there you find a detailed description of the available options.

The RGMII interface is available on the additional DHCOM-X connector of the DHCOM module.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
RGMII_RXCLK	Receive Reference Clock	1	I	SAI1_TXC	-
RGMII_RXD0	Receive Data 0	3	I	SAI1_RXD4	-
RGMII_RXD1	Receive Data 1	5	I	SAI1_RXD5	-
RGMII_RXD2	Receive Data 2	7	I	SAI1_RXD6	-
RGMII_RXD3	Receive Data 3	9	I	SAI1_RXD7	-
RGMII_RX_CTL	Receive Control	11	O	SAI1_TXFS	-
RGMII_MDIO	Management Data Input / Output	13	IO	SAI1_RXD3	-
RGMII_RST	Ethernet Reset	15	O	SAI1_RXD0	-
RGMII_WOL_INT	Wake on LAN interrupt (3V3 capable)	17	I	SAI1_TXD6	-
RGMII_TXCLK	Transmit Reference Clock	2	O	SAI1_TXD5	-
RGMII_TXD0	Transmit Data 0	4	O	SAI1_TXD0	-
RGMII_TXD1	Transmit Data 1	6	O	SAI1_TXD1	-
RGMII_TXD2	Transmit Data 2	8	O	SAI1_TXD2	-
RGMII_TXD3	Transmit Data 3	10	O	SAI1_TXD3	-
RGMII_TX_CTL	Transmit Control	12	O	SAI1_TXD4	-
RGMII_MDC	Management Data Clock	14	O	SAI1_RXD2	-
RGMII_REFCLK	Not used with i.MX8M Plus (125 MHz Clock)	16	I	-	PU
RGMII_INT	Interrupt (3V3 capable)	18	I	SAI1_RXD1	PU
VCC_RGMII_OUT	Power Supply (1V8)	20	PWR_O	-	-

Table 19: RGMII Interface Connection

7.2 USB

The DHCOM i.MX8M Plus provides two USB 3.0 Type C super-speed controllers with integrated PHY (also supported USB 2.0).

The first SOM port is named “USB OTG”, because it also offers the possibility to support a USB 2.0 OTG port.

Then second port is named “USB Host 1”.

Notes:

- The Type-C orientation selection must be handled from the USB Type-C Port Controller (TCPC). The DHCOM modules doesn’t offer a dedicated pin for this function.

- The USB 2.0 and super-speed ports must not be mixed up. USB_OTG belongs to USB_SS_1 and USB_HOST_1 belongs to USB_SS_2.

7.2.1 USB OTG / USB 3.0 port 1

This USB interface fulfils the USB 3.0 specification. It can be configured as OTG, host or device and supports all speed grades at low-speed (1.2 Mbit/s), full-speed (12 Mbit/s), high-speed (480Mbps) and super-speed (5Gbps). The interface can be used as follows.

1. USB Type-C port:

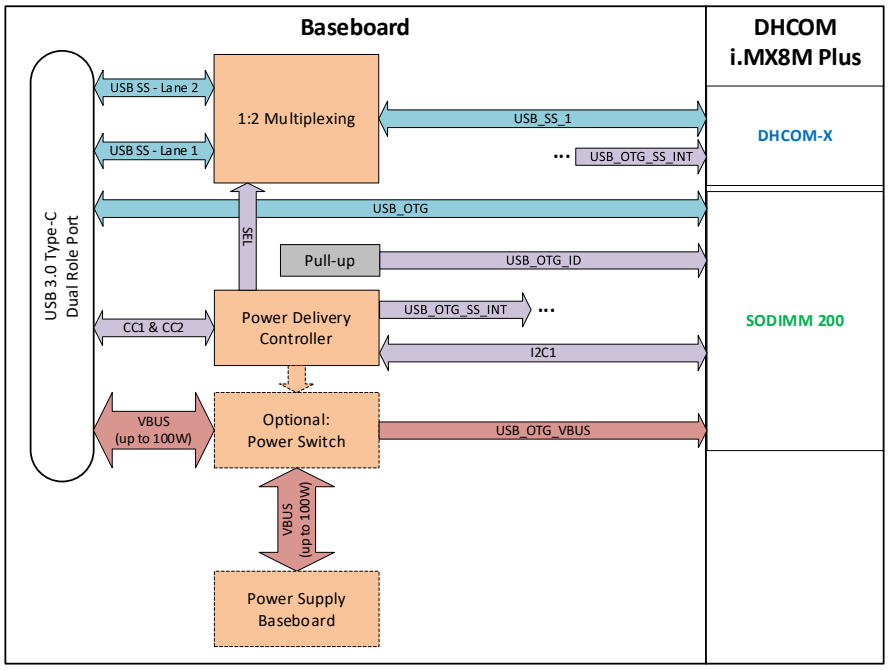

Figure 14: USB_OTG used as Type-C port

2. USB OTG port:

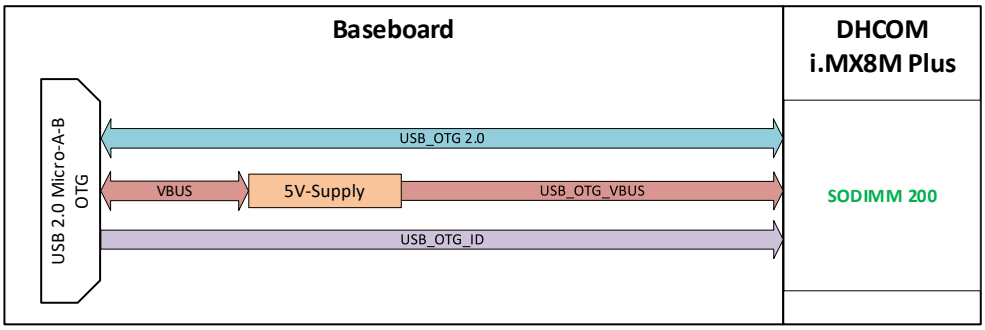

Figure 15: USB_OTG used as USB OTG port

3. USB Host 3.0 port:

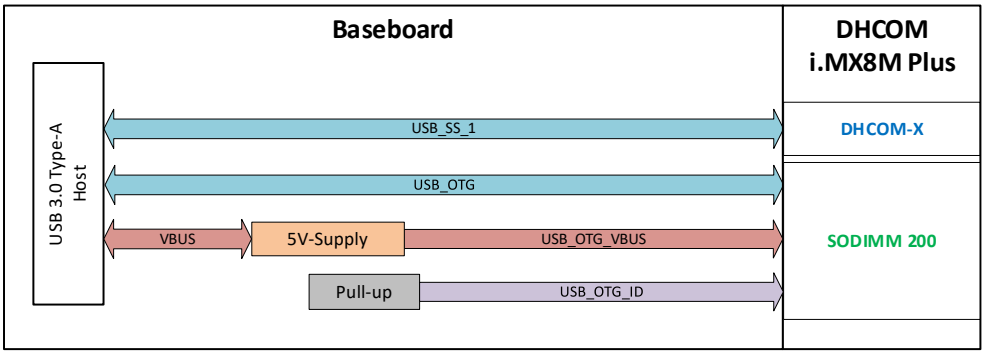

Figure 16: USB_OTG used as USB Host 3.0

4. USB Host 2.0 port:

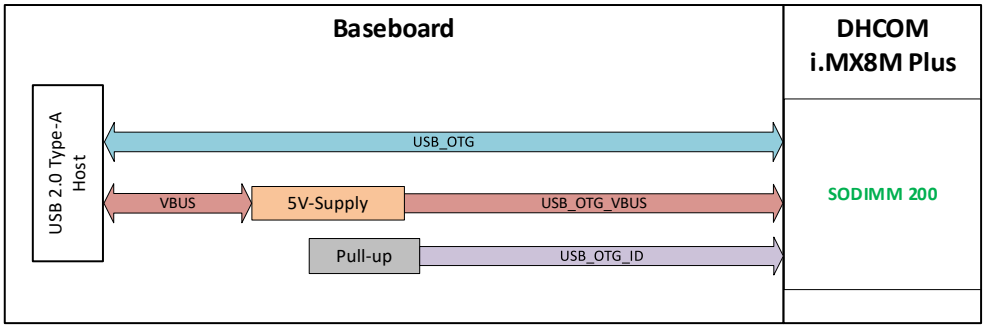

Figure 17: USB_OTG used as USB Host 2.0

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_OTG_VBUS	OTG Client: VBUS Input line OTG Host: USB bus supply voltage (reference input)	166	I	USB1_VBUS	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	USB1_ID (and I2C: 0x74; P0.6)	-
USB_OTG_D+	USB OTG differential Signal positive line	170	IO	USB1_D_P	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	IO	USB1_D_N	PD

Table 20: USB OTG

DHCOM-X pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_SS_TX1+	USB 3.0 port 1 Tx differential Signal positive line	69	O	USB1_TX_P	-
USB_SS_TX1-	USB 3.0 port 1 Tx differential Signal negative line	71	O	USB1_TX_N	-
USB_SS_RX1+	USB 3.0 port 1 Rx differential Signal positive line	73	I	USB1_RX_P	-
USB_SS_RX1-	USB 3.0 port 1 Rx differential Signal negative line	75	I	USB1_RX_N	-
USB_SS_INT	USB Type-C Port Controller (TCPC) interrupt line (3V3 capable)	77	I	SAI2_TXC	-

Table 21: "USB OTG" super-speed lanes

Notes:

- The DHCOM USB OTG port does not provide any "enable" and "over current" signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event,

the "over current" output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

- The USB OTG ID functionality of the i.MX8M Plus is broken, therefore the ID pin is additional connected to the IO expander, that the ID detection can also be handled via GPIO. (See also 7.9.3 On-module I2CTM)

7.2.2 USB Host 1 / USB 3.0 port 2

The DHCOM i.MX8M Plus module provides an USB 3.0 compliant host interface, supporting data transfers at low-speed (1.2 Mbit/s), full-speed (12 Mbit/s), high-speed (480Mbps) and super-speed (5Gbps).
The interface can be used as follows.

1. USB Host 3.0 port:

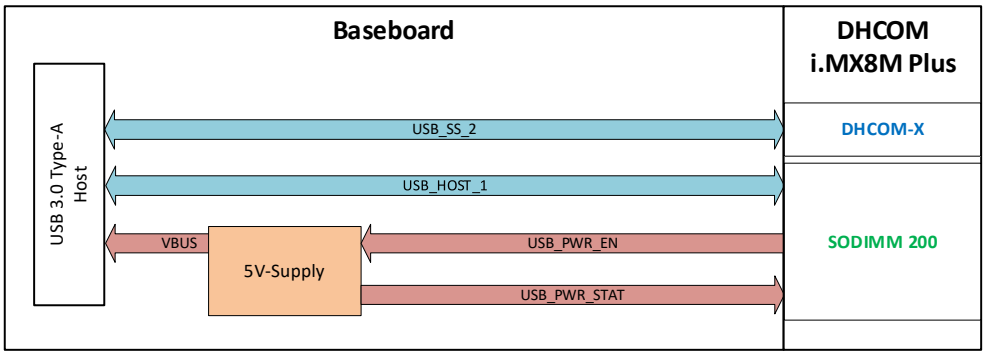

Figure 18: USB_Host 1 used as USB Host 3.0

2. USB Host 2.0 port:

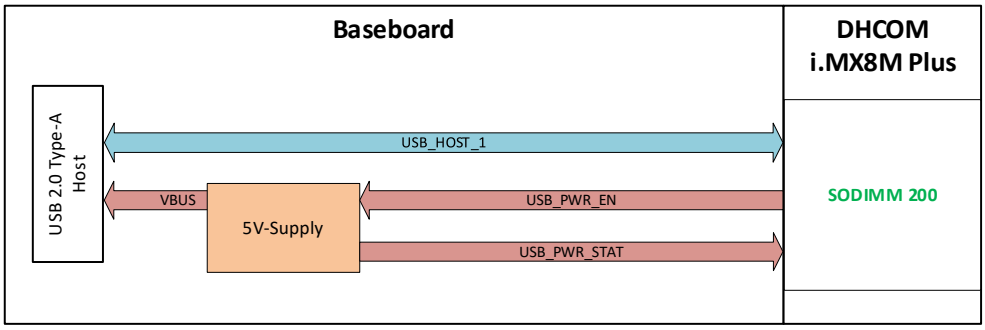

Figure 19: USB_Host 1 used as USB Host 2.0

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_PWR_STAT	USB Host over current indicator (active low)	174	I	GPIO1_IO15	-
USB_PWR_EN	USB Host power enable signal (active low)	176	O	GPIO1_IO14	-
USB_HOST_D1+	USB Host differential Signal positive line	178	IO	USB2_D_P	PD
USB_HOST_D1-	USB Host differential Signal negative line	180	IO	USB2_D_N	PD

Table 22: USB Host

DHCOM-X pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
USB_SS_TX2+	USB 3.0 port 2 Tx differential Signal positive line	70	O	USB1_TX_P	-
USB_SS_TX2-	USB 3.0 port 2 Tx differential Signal negative line	72	O	USB1_TX_N	-
USB_SS_RX2+	USB 3.0 port 2 Rx differential Signal positive line	74	I	USB1_RX_P	-
USB_SS_RX2-	USB 3.0 port 2 Rx differential Signal negative line	76	I	USB1_RX_N	-

Table 23: "USB Host 1" super-speed lanes

Note:

- The "USB Host 1" doesn't offer a dedicated USB Type-C Port Controller (TCPC) interrupt line. Therefore, a GPIO must be used, if the "USB Host 1" is used for Type-C connection.

7.3 PCIe

The DHCOM i.MX8M Plus module provides PCIe interface, which is designed to be compatible with PCIe specification Gen3 x1 lane and supports the PCI Express 1.1/2.0/3.0 standards.

Notes:

- It is recommended to use an external PCIe clock generator to generate the 100MHz reference clock. The clock can be feeded back to the SoM by the PCIE_REFCLK pins.
- For a regular PCIe slot connector, no additional decoupling capacitors are permitted to be placed on the carrier board in the RX, TX, and reference clock lines. The decoupling capacitors are located on the SoM and the PCIe card.

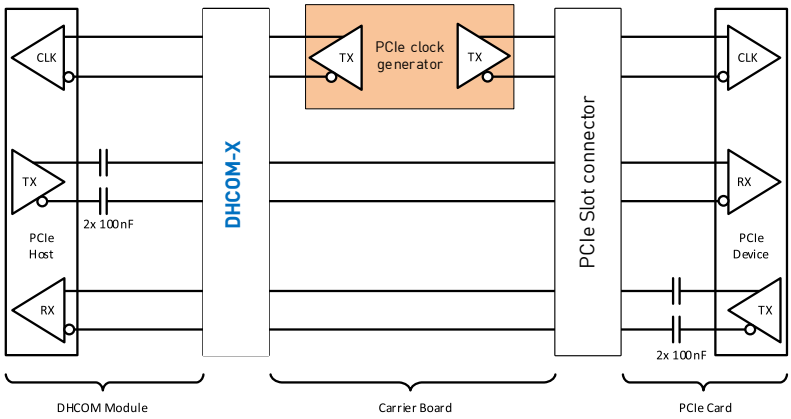

Figure 20: PCIe example

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
PCIE_RX+	PCIe receive data positive	27	I	PCIE_RXN_P	-
PCIE_RX-	PCIe receive data negative	29	I	PCIE_RXN_N	-
PCIE_TX+	PCIe transmit data positive	31	O	PCIE_TXN_P	-
PCIE_TX-	PCIe transmit data negative	33	O	PCIE_TXN_N	-
PCIE_REFCLK+	PCIe 100MHz reference clock output positive	30	IO	PCIE_REF_PAD_CLK_P	-
PCIE_REFCLK-	PCIe 100MHz reference clock output negative	32	IO	PCIE_REF_PAD_CLK_N	-
PCIE_WAKE	PCIe wake signal (active low)	34	I	SAI2_TXD0	PU

Table 24: PCIe Interface

7.4 ADC

The DHCOM i.MX8M Plus module feature up to four analog input channels. On the SoM the AD-converter ADS1015 from TI is used, which is connected via I2C™ with the i.MX8M Plus processor. This part offers the following features:

- 12-Bit Delta-Sigma ADC.
- Integrated low-drift voltage reference.
- Wide input voltage range. Selectable from ±256 mV to ±6.144 V.
- Programmable Data Rate: 128 SPS to 3.3 kSPS
- Continuous-Conversion Mode or Single-shot mode

The I2C™ device address of the touch controller is 0x48. (See also 7.9.3 On-module I2CTM)

FSR	LSB SIZE
±6.144 V[1]	3 mV
±4.096 V[1]	2 mV
±2.048 V	1 mV
±1.024 V	0.5 mV
±0.512 V	0.25 mV
±0.256 V	0.125 mV

Table 25: ADC Full-Scale Range and Corresponding LSB Size

[1] In case of the DHCOM i.MX8M Plus a VDD supply voltage of 3.3V is used, the ±6.144 V and ±4.096 V ranges allow input voltages to extend up to the supply. In this case the supply voltage is less than the full-scale range, a full-scale ADC output code cannot be obtained. For example, with VDD = 3.3 V and FSR = ±4.096 V, only signals up to VIN = ±3.3 V can be measured. The code range that represents voltages |VIN| > 3.3 V is not used in this case.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Range	Not used
AD0_IN	Analog input channel 0	8	AIN	-	0-3.3V	-
AD1_IN	Analog input channel 1	6	AIN	-	0-3.3V	-
AD2_IN	Analog input channel 2	4	AIN	-	0-3.3V	-
AD3_IN	Analog input channel 3	2	AIN	-	0-3.3V	-

Table 26: Analog inputs/outputs

Notes:

- The ALERT/RDY pin is connected to the IC2 IO Expander: I2C: 0x74; P0.7 (See also 7.9.3 On-module I2CTM)
- DHCOM analog inputs are only available if option [–ADC] is selected in the specific variant.

7.5 Touch controller

The DHCOM i.MX8M Plus module is equipped with a 4-Wire 12-bit resistive Touch Controller (Texas Instruments TSC2014), which is connected via I2C™ with the i.MX8M Plus processor.

The I2C™ device address of the touch controller is 0x49. (See also 7.9.3 On-module I2CTM)

Notes:

- The resistive touch controller is only available if option [–T] is selected in the specific variant.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
TSPX	Resistive Touch: 4 wire (X +)	12	AINOUT	-	PD
TSMX	Resistive Touch: 4 wire (X -)	14	AINOUT	-	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	AINOUT	-	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	AINOUT	-	PD

Table 27: Touch controller connections

7.6 Audio / I2S

On the DHCOM i.MX8M Plus module the SAI can be used as I2S interfaces, therefore it is connected to the I2S pins on the SODIMM-200 connector. The interface supports either master or slave mode. In many use cases the master configuration is needed. Therefore, it is the preferred configuration. The following signals are used for a simple I2S interface:

Note:

- The DHCOM I2S interface is connected to the i.MX8M Plus SAI3 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2S_RXFS	Receive Frame sync signal	1	I	SAI3_RXFS	-
I2S_RXD	Data receive signal	5	I	SAI3_RXD	-
I2S_RXC	Receive clock signal	7	I	SAI3_RXC	-
I2S_TXFS	Transmit Frame sync signal	11	O	SAI3_TXFS	-
I2S_TXD	Data transmit signal	15	O	SAI3_TXC	-
I2S_TXC	Transmit clock signal	13	O	SAI3_TXD	-

Table 28: Audio interface

7.7 UART

The DHCOM i.MX8M Plus module provides three UART interfaces on the SODIMM connector. The DHCOM UART ports UART1 and UART2 are both implemented with CTS/RTS flow control. The DHCOM UART3 is used as UART interface without flow control.

The maximum transfer rate is 4Mbit/s.

7.7.1 UART 1

Notes:

- The DHCOM UART 1 interface is connected to the i.MX8M Plus UART1 interface.
- UART CTS and RTS signals are only available if CAN port 2 is not available. This means a module variant without option [–CAN2] must be used to support hardware handshake with DHCOM UART 1.

- It is essential to always create a possible connection to DHCOM UART 1, since the bootloader and Linux command line can be operated by default with the UART 1. A minimum connection possibility should be made available via solder pads.
- For RS-485 connection use UART1 RTS as direction control pin and UART1 CTS to switch on and off the echo functionality.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART1_CTS	UART clear to send	24	I	SAI2_RXD0	-
UART1_RTS	UART request to send	26	O	SAI2_TXFS	-
UART1_RX	UART receive data line	32	I	SAI2_RXC	-
UART1_TX	UART transmit data line	34	O	SAI2_RXFS	-

Table 29: UART 1

7.7.2 UART 2

Notes:

- The DHCOM UART 2 interface is connected to the i.MX8M Plus UART3 interface.
- For RS-485 connection use UART2 RTS as direction control pin and UART2 CTS to switch on and off the echo functionality.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART2_CTS	UART clear to send	31	I	ECSPI1_SS0	-
UART2_RTS	UART request to send	33	O	ECSPI1_MISO	-
UART2_RX	UART receive data line	35	I	ECSPI1_SCLK	-
UART2_TX	UART transmit data line	37	O	ECSPI1_MOSI	-

Table 30: UART 2

7.7.3 UART 3

Notes:

- The DHCOM UART 3 interface is connected to the i.MX8M Plus UART4 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
UART3_RX	UART receive data line	23	I	UART4_RX	-
UART3_TX	UART transmit data line	25	O	UART4_TX	-

Table 31: UART 3

7.8 SPI

The DHCOM i.MX8M Plus module provides two SPI interfaces, which can be configured in full-duplex enhanced Synchronous Serial Interface mode, with data rate up to 52 Mbit/s. The interface also supports both Master and Slave mode.

7.8.1 SPI 1

Notes:

- The DHCOM SPI 1 interface is connected to the i.MX8M Plus ECSPI1 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SPI1_CS0	Slave select signal	177	O	I2C2_SDA	-
SPI1_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	I2C1_SCL	-
SPI1_MISO	SPI receive data line	181	I	I2C2_SCL	-
SPI1_MOSI	SPI transmit data line	183	O	I2C1_SDA	-

Table 32: SPI 1

7.8.2 SPI 2

Notes:

- The DHCOM SPI 2 interface is connected to the i.MX8M Plus ECSPI2 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SPI2_CS0	Slave select signal	155	O	ECSPI2_SS0	-
SPI2_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	157	IO	ECSPI2_SCLK	-
SPI2_MISO	SPI receive data line	159	I	ECSPI2_MISO	-
SPI2_MOSI	SPI transmit data line	161	O	ECSPI2_MOSI	-

Table 33: SPI 2

7.9 I2C™

The DHCOM i.MX8M Plus module provides two external I2C™ interfaces on the SODIMM connector and one on-module I2C™ interface to connect several peripherals (e.g. PMIC, RTC; ...).
The I2C interfaces support standard (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s).

Notes:

- The pull-up resistors required according to the I2C™ specification are already fitted on the module. For detailed information about I2C™, reference is made to the specification (Philips Semiconductor): http://www.nxp.com
- The waveform quality depends also on the connected parts at the mainboard. Therefore, depending on the mainboard circuit, additional pull-up resistors may be useful.

7.9.1 I2C 1

Notes:

- The DHCOM I2C 1 interface is connected to the i.MX8M Plus I2C5 interface.

- DHCOM I2C 1 can also be used as HDMI_DDC interface. Depending on the HDMI driver, the dedicated HDMI_DDC or the general-purpose I2C is used.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2C1_CLK	I²C clock line	182	IO	HDMI_DDC_SCL	-
I2C1_DAT	I²C data line	184	IO	HDMI_DDC_SDA	-

Table 34: I2C 1

7.9.2 I2C 2

Notes:

- The DHCOM I2C 2 interface is connected to the i.MX8M Plus I2C4 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
I2C2_CLK	I²C clock line	158	IO	I2C4_SCL	-
I2C2_DAT	I²C data line	160	IO	I2C4_SDA	-

Table 35: I2C 2

7.9.3 On-module I2C™

The onboard I2C interface is used to connect the following I2C devices:

Device		Address (7bit)
MIPI-DSI to RGB/DP bridge	Toshiba TC9595XBG	0x0F
PMIC	NXP PCA9450CHN	0x25
AD-converter	TI ADS1015	0x48
Resistiv -touch-controller	TI TSC2014	0x49
EEPROM ENET_QOS	Microchip 24AA025E48T-I/OT	0x50
RTC	MicroCrystal RV-3032-C7	0x51
RTC (optional)	MicroCrystal RV-3028-C7	0x52
EEPROM ENET1	Microchip 24AA025E48T-I/OT	0x53
IO-Expander	NXP PCA9539AHF	0x74

Table 36: Onboard I2C devices

Notes:

- The onboard I2C interface is connected to the i.MX8M Plus I2C3 interface.
- The following CPU pins are used: I2C3_SDA and I2C3_SCL

7.10 CAN

The DHCOM i.MX8M Plus module supports both CAN modules (FlexCAN1 and FlexCAN2) of the i.MX8M Plus. The FlexCAN controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.

7.10.1 CAN 1

Note: The DHCOM CAN 1 interface is connected to the i.MX8M Plus FlexCAN1 interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
CAN_TX	CAN transmit data line	27	O	SPDIF_TX	-
CAN_RX	CAN receive data line	29	I	SPDIF_RX	-

Table 37: CAN 1

7.10.2 CAN 2

Notes:

- The DHCOM CAN 2 interface is connected to the i.MX8M Plus FlexCAN2 interface.
- DHCOM CAN 2 is only available if option [–CAN2] is selected in the specific variant. Then DHCOM UART1 hardware handshake (RTS and CTS) is not available.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
CAN2_TX	CAN transmit data line	24	O	UART3_RXD	-
CAN2_RX	CAN receive data line	26	I	UART3_TXD	-

Table 38: CAN 2

7.11 Display

The DHCOM i.MX8M Plus offers several display interfaces and mounting options.

See also 2.1 Ordering options and configuration.

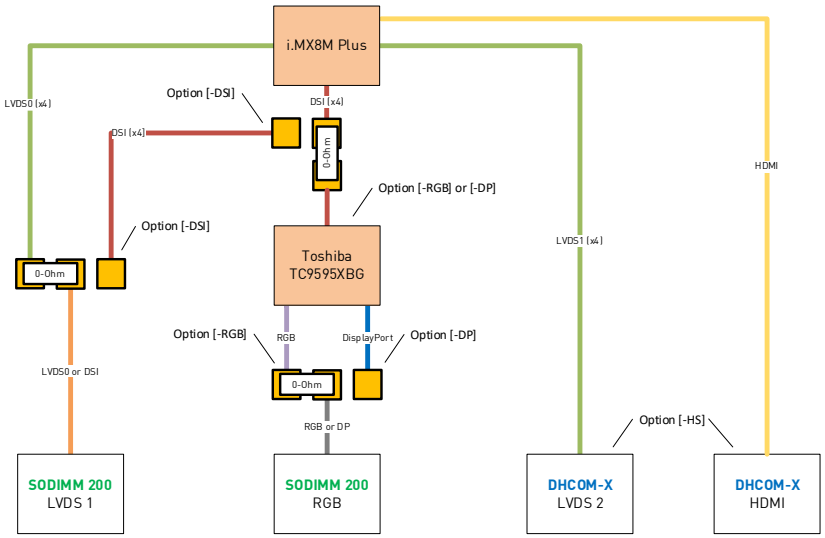

Figure 21: Display interface Options

The i.MX8M Plus LCDIF display controller support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.

- One LCDIF drives MIPI DSI, up to UWHD and WUXGA
- One LCDIF drives LVDS Tx, up to 1920x1080p60
- One LCDIF drives HDMI Tx, up to 4kp30

7.11.1 RGB

The i.MX8M Plus does NOT provide a native 24-bit parallel digital RGB (Red, Green, Blue) interface. Therefore, DH electronics used on the DHCOM i.MX8M Plus the Toshiba bridge device TC9595XBG to offer the parallel RGB interface with the System on Module.

This MIPI®-DSI to RGB bridge delivers all signals for connecting a LCD and TFT panel with maximum resolution WXGA (1280x800 or 1366x768) and pixel rate up to 100 MHz.

Notes:

- The Interface only supports 1V8 IO voltage. Therefore, Vdisp references to 1V8.
- The RGB interface pins are shared with DisplayPort™ pins. This means, either one or the other is possible. Please have a look at Figure 21: Display interface Options.
- The RGB interface is only available if option [–RGB] is selected and [-DSI] is NOT selected in the specific variant.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-	-
LC_R0	LCD display data red 0	76	O	-	-
LC_R1	LCD display data red 1	78	O	-	-
LC_R2	LCD display data red 2	49	O	-	-
LC_R3	LCD display data red 3	51	O	-	-
LC_R4	LCD display data red 4	53	O	-	-
LC_R5	LCD display data red 5	55	O	-	-
LC_R6	LCD display data red 6	57	O	-	-
LC_R7	LCD display data red 7	59	O	-	-
LC_G0	LCD display data green 0	80	O	-	-
LC_G1	LCD display data green 1	82	O	-	-
LC_G2	LCD display data green 2	61	O	-	-
LC_G3	LCD display data green 3	63	O	-	-
LC_G4	LCD display data green 4	65	O	-	-
LC_G5	LCD display data green 5	67	O	-	-
LC_G6	LCD display data green 6	69	O	-	-
LC_G7	LCD display data green 7	71	O	-	-
LC_B0	LCD display data blue 0	84	O	-	-
LC_B1	LCD display data blue 1	86	O	-	-
LC_B2	LCD display data blue 2	73	O	-	-
LC_B3	LCD display data blue 3	75	O	-	-
LC_B4	LCD display data blue 4	77	O	-	-
LC_B5	LCD display data blue 5	79	O	-	-
LC_B6	LCD display data blue 6	81	O	-	-
LC_B7	LCD display data blue 7	83	O	-	-
LC_EN	LCD display data enable	85	O	-	-
LC_VSYNC	LCD frame or vertical sync. pulse	87	O	-	-
LC_HSYNC	LCD line or horizontal sync. pulse	89	O	-	-
LC_PCLK	LCD pixel clock	91	O	-	-
GPIO_PWM	LCD contrast (only if PWM is not used)	100	O	GPIO1_IO1	-

Table 39: RGB

7.11.2 MIPI®-DSI

The DHCOM i.MX8M Plus offers the MIPI® DSI interface, which is part of a group of communication protocols defined by the MIPI® Alliance. The interface uses the MIPI D-PHY for the physical layer, compatible with the version 1.2 specifications. The maximum data transfer per lane is 1.5Gbps. Bi-directional data transmission is available on lane 0. Resolutions up 1920x1080p60 with 24-bit RGB are supported.

Notes:

- The MIPI® DSI interface pins are shared with LVDS and also with RGB and DisplayPort™. This means, either one or the other is possible. Please have a look at Figure 21: Display interface Options.
- The MIPI® DSI interface is only available if option [–DSI] is selected in the specific variant. Then MIPI® DSI interface is connected to the original DHCOM LVDS connections.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
DSI_D0_P / (LVDS_TX0+)	DSI data0 differential signal positive line	88	IO	MIPI_DSI1_D0_P	-
DSI_D0_N / (LVDS_TX0-)	DSI data0 differential signal negative line	90	IO	MIPI_DSI1_D0_N	-
DSI_D1_P / (LVDS_TX1+)	DSI data1 differential signal positive line	92	O	MIPI_DSI1_D1_P	-
DSI_D1_N / (LVDS_TX1-)	DSI data1 differential signal negative line	94	O	MIPI_DSI1_D1_N	-
DSI_D2_P / (LVDS_TX2+)	DSI data2 differential signal positive line	93	O	MIPI_DSI1_D2_P	-
DSI_D2_N / (LVDS_TX2-)	DSI data2 differential signal negative line	95	O	MIPI_DSI1_D2_N	-
DSI_D3_P / (LVDS_TX3+)	DSI data3 differential signal positive line	96	O	MIPI_DSI1_D3_P	-
DSI_D3_N / (LVDS_TX3-)	DSI data3 differential signal negative line	98	O	MIPI_DSI1_D3_N	-
DSI_CK_P / (LVDS_CLK+)	DSI clock differential signal positive line	97	O	MIPI_DSI1_CLK_P	-
DSI_CK_N / (LVDS_CLK-)	DSI clock differential signal negative line	99	O	MIPI_DSI1_CLK_N	-

Table 40: MIPI DSI

7.11.3 LVDS

The DHCOM i.MX8M Plus features one dual-channel LVDS interface that can be configured for a single or dual-channel mode with 18 and 24-bit.

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (80MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel. The dual-channel LVDS interface can support resolutions up to 1920x1080 @60fps (160MHz pixel clock maximum).

Notes:

- The LVDS channel 1 interface pins are shared with MIPI® DSI. This means, either one or the other is possible. Please have a look at Figure 21: Display interface Options.
- The LVDS channel 1 interface is only available if option [–DSI] is NOT selected in the specific variant.
- The LVDS channel 2 interface is only available if option [–HS] is selected in the specific variant.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
LVDS_TX0+	LVDS0 data 0 output positive line	88	O	LVDS0_D0_P	-
LVDS_TX0-	LVDS0 data 0 output negative line	90	O	LVDS0_D0_N	-
LVDS_TX1+	LVDS0 data 1 output positive line	92	O	LVDS0_D1_P	-
LVDS_TX1-	LVDS0 data 1 output negative line	94	O	LVDS0_D1_N	-
LVDS_TX2+	LVDS0 data 2 output positive line	93	O	LVDS0_D2_P	-
LVDS_TX2-	LVDS0 data 2 output negative line	95	O	LVDS0_D2_N	-
LVDS_TX3+	LVDS0 data 3 output positive line	96	O	LVDS0_D3_P	-
LVDS_TX3-	LVDS0 data 3 output negative line	98	O	LVDS0_D3_N	-
LVDS_CLK+	LVDS0 clock output positive line	97	O	LVDS0_CLK_P	-
LVDS_CLK-	LVDS0 clock output negative line	99	O	LVDS0_CLK_N	-

Table 41: LVDS channel 1

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
LVDS2_TX0+	LVDS1 data 0 output positive line	60	O	LVDS1_D0_P	-
LVDS2_TX0-	LVDS1 data 0 output negative line	62	O	LVDS1_D0_N	-
LVDS2_TX1+	LVDS1 data 1 output positive line	64	O	LVDS1_D1_P	-
LVDS2_TX1-	LVDS1 data 1 output negative line	66	O	LVDS1_D1_N	-
LVDS2_TX2+	LVDS1 data 2 output positive line	59	O	LVDS1_D2_P	-
LVDS2_TX2-	LVDS1 data 2 output negative line	61	O	LVDS1_D2_N	-
LVDS2_TX3+	LVDS1 data 3 output positive line	63	O	LVDS1_D3_P	-
LVDS2_TX3-	LVDS1 data 3 output negative line	65	O	LVDS1_D3_N	-
LVDS2_CLK+	LVDS1 clock output positive line	55	O	LVDS1_CLK_P	-
LVDS2_CLK-	LVDS1 clock output negative line	57	O	LVDS1_CLK_N	-

Table 42: LVDS channel 2

7.11.4 HDMI

The DHCOM i.MX8M Plus provides a High-Definition Multimedia interface (HDMI) with the following characteristics:

- HDMI 2.0a Tx supporting one display
  - Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30
  - Pixel clock up to 297 MHz
- Audio support
  - 32-channel audio output support
  - 1 SPDIF audio eARC input support

Notes:

- DHCOM I2C 1 can be used as HDMI_DDC interface. Depending on the HDMI driver, the dedicated HDMI_DDC or the general-purpose I2C is used.
- The HDMI interface is only available if option [–HS] is selected in the specific variant.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
HDMI_D0+	HDMI differential data lane 0 positive	48	O	HDMI_TX0_P	-
HDMI_D0-	HDMI differential data lane 0 negative	50	O	HDMI_TX0_N	-
HDMI_D1+	HDMI differential data lane 1 positive	52	O	HDMI_TX1_P	-
HDMI_D1-	HDMI differential data lane 1 negative	54	O	HDMI_TX1_N	-
HDMI_D2+	HDMI differential data lane 2 positive	47	O	HDMI_TX2_P	-
HDMI_D2-	HDMI differential data lane 2 negative	49	O	HDMI_TX2_N	-
HDMI_CLK+	HDMI differential clock positive	43	O	HDMI_TXC_P	-
HDMI_CLK-	HDMI differential clock negative	45	O	HDMI_TXC_N	-
HDMI_CEC	HDMI Consumer Electronic Control.	51	IO	HDMI_CEC	-
HDMI_HPD	HDMI hot plug detect	56	I	HDMI_HPD	-

Table 43: HDMI

7.11.5 DisplayPort™

The i.MX8M Plus does NOT provide a native DisplayPort™ interface. Therefore, DH electronics used on the DHCOM i.MX8M Plus the Toshiba bridge device TC9595XBG to offer the DisplayPort™ interface with the System on Module.

This MIPI®-DSI to dual-lane DisplayPort™ interface offers the following features:

- High speed serial bridge chip using VESA® DisplayPort™ 1.1a Standard.
- Resolution up to WUXGA (1920x1200) at 24bit, 60 fps.
- Supports one dual-lane DisplayPort™ port for high bandwidth applications
- Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2V
- Support of pre-emphasis levels of 0, 3.5dB and 6dB.
- AUX channel supported at 1 Mbps.
- HPD support through GPIO based interrupts
- Enhanced mode supported for content protection.

Notes:

- The DisplayPort™ interface is shared with the RGB pins. This means, either one or the other is possible. Please have a look at Figure 21: Display interface Options.
- The DisplayPort™ interface is only available if option [–DP] is selected and [-DSI] is NOT selected in the specific variant.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
DPLNM0 / (LC_R2)	DisplayPort™ output lane0 main link neg.	49	O	-	-
DPLNP0 / (LC_R3)	DisplayPort™ output lane0 main link pos.	51	O	-	-
DPLNM1 / (LC_R4)	DisplayPort™ output lane1 main link neg.	53	O	-	-
DPLNP1 / (LC_R5)	DisplayPort™ output lane1 main link pos.	55	O	-	-

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
DPAUXM / (LC_R6)	DisplayPort™ output AUX channel neg.	57	O	-	-
DPAUXP / (LC_R7)	DisplayPort™ output AUX channel pos.	59	O	-	-
HPD / (LC_G2)	TC9595XBG gpio1 / hot plug detect	61	O	-	-
gpio0 / (LC_G3)	TC9595XBG gpio0	63	O	-	-

Table 44: DisplayPort™

7.12 MIPI®-CSI2

The DHCOM i.MX8M Plus supports two quad lane MIPI® CSI-2 interfaces for connecting compatible cameras. The interface is compatible with single, dual, and quad lane CSI cameras, uses MIPI® D-PHY as the physical layer and supports RGB, YUV, and RAW color space definitions.

Features:

- Scalable data lane support, 1 to 4 Data Lanes
  - For single Camera, MIPI® CSI-2 CSI1 can support up to 400/500 MHz pixel clock in the Nominal/Overdrive mode.
  - For single Camera, MIPI® CSI-2 CSI2 can support up to 277 MHz pixel clock.
  - For dual Camera, both MIPI® CSI-2 can support up to 266 MHz pixel clock.
- MIPI® CSI-2 specification V1.3 (except for the C-PHY feature)
- MIPI® D-PHY specification V1.2
- Supported primary and secondary image format: YUV420, YUV420 (legacy), YUV420 (CSPS), YUV 422 (8-bit and 10-bit), RGB565, RGB666, RGB888, RAW6, RAW7, RAW8, RAW10, RAW12, and RAW14
- 2x ISP supporting 375 Mpixel/s aggregate performance and up to 3-exposure HDR processing.
  - When one camera is used, support up to 12MP@30fps or 4kp45
  - When two cameras are used, each supports up to 1080p80

The DHCOM i.MX8M Plus offers several MIPI® CSI-2 interface and mounting options:

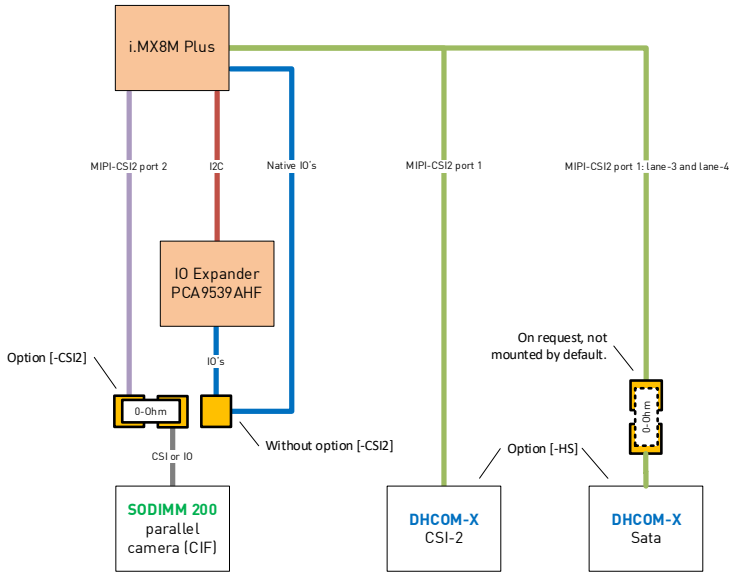

Figure 22: MIPI® CSI-2 interface options

7.12.1 CSI 1

The DHCOM Standard offers a dual-lane MIPI® CSI-2 interface on the DHCOM-X connector. Therefore, the first port of the i.MX8M Plus MIPI® CSI-2 interface is connected as dual-lane port, which is sufficient for many applications. But the additional lanes 3 and 4 are optional connected to the Sata interface. This can be ordered on request if needed.

Please have a look at Figure 22: MIPI® CSI-2 interface options.

Notes:

- The MIPI® CSI-2 port 1 interface is only available if option [–HS] is selected in the specific variant.
- The usage of the additional lanes 3 and 4 at the Sata interface break's the compatibility with the DHCOM standard.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
CSI_D0+	CSI received data 0 positive	38	I	MIPI_CSI1_D0_P	-
CSI_D0-	CSI received data 0 negative	40	I	MIPI_CSI1_D0_N	-
CSI_D1+	CSI received data 1 positive	42	I	MIPI_CSI1_D1_P	-
CSI_D1-	CSI received data 1 negative	44	I	MIPI_CSI1_D1_N	-
CSI_CLK+	CSI reference clock positive	37	I	MIPI_CSI1_CLK_P	-
CSI_CLK-	CSI reference clock negative	39	I	MIPI_CSI1_CLK_N	-
SATA_TX+ / (CSI_D3+)	On request!!! (CSI received data 3 positive)	24	O / I	MIPI_CSI1_D3_P	-
SATA_TX- / (CSI_D3-)	On request!!! (CSI received data 3 negative)	26	O / I	MIPI_CSI1_D3_N	-
SATA_RX+ / (CSI_D2+)	On request!!! (CSI received data 2 positive)	21	I	MIPI_CSI1_D2_P	-
SATA_RX- / (CSI_D2-)	On request!!! (CSI received data 2 negative)	23	I	MIPI_CSI1_D2_N	-

Table 45: MIPI® CSI-2 port 1

7.12.2 CSI 2

The DHCOM Standard offers on the SODIMM-200 connector only the parallel camera interface (CIF). With the DHCOM i.MX8M Plus, the second MIPI® CSI-2 interface is optional connected to the CIF interface pins.

Please have a look at Figure 22: MIPI® CSI-2 interface options.

Notes:

- The MIPI® CSI-2 interface port 2 is only available if option [–CSI2] is selected in the specific variant.

DHCOM pin name	Description	DHCOM-X pin number	IO Type	CPU ball name	Not used
CSIx_#RST / (GPIO_J or CIF_HSYNC)	Camera Reset	74	O	GPIO1_IO06	-
CSIx_PWDN / (GPIO_K or CIF_PCLK)	Camera power-down	72	O	SD1_STROBE	-
CSI2_SYNC / (GPIO_L or CIF_MCLK)	Camera sync port 2	70	I	GPIO1_IO07	-
CSIx_MCLK / (GPIO_M or CIF_VSYNC)	Camera master clock	68	O	CLKOUT1	-
CSI2_D3- / (GPIO_N or CIF_D9)	CSI port 2 received data 3 negative	66	IO	MIPI_CSI2_D3_N	-
CSI2_D3+ / (GPIO_O or CIF_D8)	CSI port 2 received data 3 positive	64	IO	MIPI_CSI2_D3_P	-
CSI2_D2- / (GPIO_P or CIF_D7)	CSI port 2 received data 2 negative	62	IO	MIPI_CSI2_D2_N	-
CSI2_D2+ / (GPIO_Q or CIF_D6)	CSI port 2 received data 2 positive	60	IO	MIPI_CSI2_D2_P	-
CSI2_D1- / (GPIO_R or CIF_D5)	CSI port 2 received data 1 negative	58	IO	MIPI_CSI2_D1_N	-
CSI2_D1+ / (GPIO_S or CIF_D4)	CSI port 2 received data 1 positive	56	IO	MIPI_CSI2_D1_P	-
CSI2_D0- / (GPIO_T or CIF_D3)	CSI port 2 received data 0 negative	54	IO	MIPI_CSI2_D0_N	-
CSI2_D0+ / (GPIO_U or CIF_D2)	CSI port 2 received data 0 positive	52	IO	MIPI_CSI2_D0_P	-
CSI2_CLK- / (GPIO_V or CIF_D1)	CSI port 2 reference clock negative	50	IO	MIPI_CSI2_CLK_N	-
CSI2_CLK+ / (GPIO_W or CIF_D0)	CSI port 2 reference clock positive	48	IO	MIPI_CSI2_CLK_P	-

Table 46: MIPI® CSI-2 port 2

7.13 PWM

The DHCOM i.MX8M Plus enables the connection to Pulse Width Modulation (PWM) output.

The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Notes:

- The PWM output SODIMM pin 100 is typically used to control the Display backlight contrast.
- The DHCOM PWM interface is connected to the i.MX8M Plus PWM1_OUTinterface.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
GPIO_PWM	PWM channel (only if LCD contrast is not used)	100	O	GPIO1_IO01	-

Table 47: PWM

7.14 GPIOs

The DHCOM i.MX8M Plus module provides several GPIO pins on the SODIMM-200 socket.

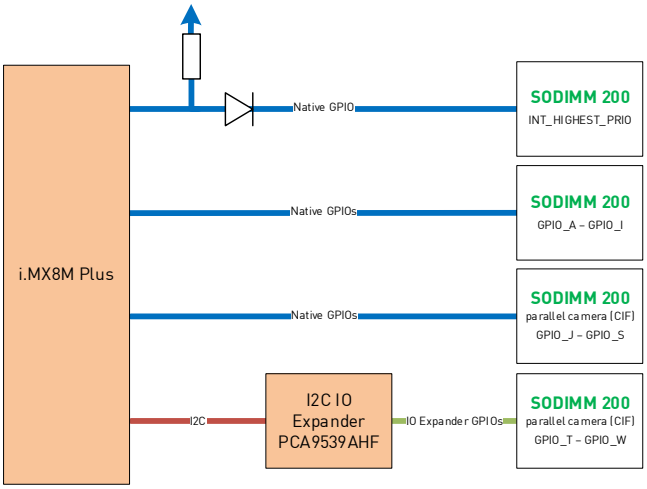

Figure 23: GPIO's

Notes:

- Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHCOM standard.
- The DHCOM camera interface can also be used as alternative GPIO bank, if the camera interface is not needed.
- The GPIO_M to GPIO_W are only available if the option [-CSI2] is not selected.
- GPIO_T to GPIO_W are not native i.MX8M Plus GPIO's. These pins are realized with I2C IO expander. (See also 7.9.3 On-module I2CTM)
- GPIO_A to GPIO_I and INT_HIGHEST_PRIORITY belongs to VIO_OUT. GPIO_J to GPIO_W belongs to VCAM_OUT. But in case of the DHCOM i.MX8M Plus module both voltage levels are 3V3.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	IO	SD2_WP	PU
GPIO _A	General Purpose I/O	154	IO	GPIO1_IO09	-
GPIO _B	General Purpose I/O	156	IO	GPIO1_IO08	-
GPIO _C	General Purpose I/O	162	IO	SAI3_MCLK	-
GPIO _D	General Purpose I/O	163	IO	SAI2_MCLK	-
GPIO _E	General Purpose I/O	164	IO	UART1_RXD	-
GPIO _F	General Purpose I/O	165	IO	UART1_TXD	-

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
GPIO _G	General Purpose I/O	167	IO	GPIO1_IO00	-
GPIO _H	General Purpose I/O	173	IO	GPIO1_IO11	-
GPIO _I	General Purpose I/O	175	IO	GPIO1_IO05	-
VIO_OUT	Voltage for external Level-Shifter	152	PWR_O	-	-
GPIO_J (or CIF_HSYNC)	General Purpose I/O	74	IO	GPIO1_IO06	-
GPIO_K (or CIF_PCLK)	General Purpose I/O	72	IO	SD1_STROBE	-
GPIO_L (or CIF_MCLK)	General Purpose I/O	70	IO	GPIO1_IO07	-
GPIO_M (or CIF_VSYNC)	General Purpose I/O	68	IO	SPDIF_EXT_CLK	-
GPIO_N (or CIF_D9)	General Purpose I/O	66	IO	SD1_DATA7	-
GPIO_O (or CIF_D8)	General Purpose I/O	64	IO	SD1_DATA6	-
GPIO_P (or CIF_D7)	General Purpose I/O	62	IO	SD1_RESET_B	-
GPIO_Q (or CIF_D6)	General Purpose I/O	60	IO	GPIO1_IO13	-
GPIO_R (or CIF_D5)	General Purpose I/O	58	IO	GPIO1_IO12	-
GPIO_S (or CIF_D4)	General Purpose I/O	56	IO	GPIO1_IO10	-
GPIO_T (or CIF_D3)	General Purpose I/O	54	IO	- (I2C: 0x74; P1.3)	-
GPIO_U (or CIF_D2)	General Purpose I/O	52	IO	- (I2C: 0x74; P1.2)	-
GPIO_V (or CIF_D1)	General Purpose I/O	50	IO	- (I2C: 0x74; P1.1)	-
GPIO_W (or CIF_D0)	General Purpose I/O	48	IO	- (I2C: 0x74; P1.0)	-
Vcam_OUT	Voltage for external Level-Shifter	102	PWR_O	-	-

Table 48: GPIO's

7.15 SD/MMC

The i.MX8M Plus SoC provides three SDIO interfaces. One is used internally for the eMMC Flash. A second one is available on the SODIMM-200 connector, if a module without onboard microSD socked is used. The third interface is used for the Wi-Fi® and Bluetooth module.

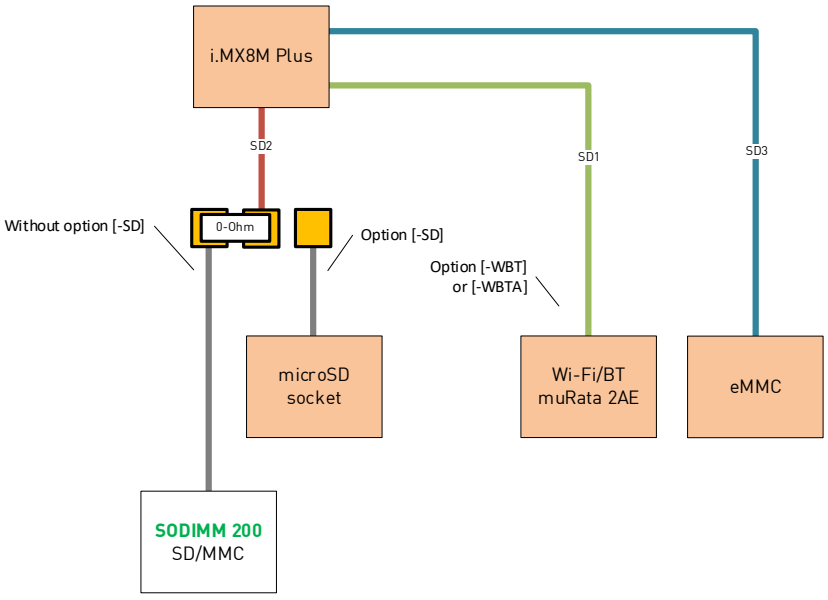

Figure 24: SD/MMC Interfaces

Features:

- SD/SDIO 3.01 compliance with 200 MHz SDR signaling to support up to 100MB/sec.
- Support for SDXC (extended capacity).
- Supports SD UHS-I mode (up to 208MHz) with a 1.8V IO voltage level.
- 3.3V and 1.8V IO voltage mode supported.

Notes:

- The DHCOM SD interface is only available if option [-SD] is not selected.
- USDHC2 of the i.MX8M Plus is used for the external SDIO interface.
- SD_DETECT is not directly connected to the SD2_CD_B pin. An inverter is included to adjust DHCOM and internal card detect level.

SODIMM pin name	Description	SODIMM pin number	IO Type	CPU ball name	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	SD2_CLK	-
SD_CMD	SD/SDIO/MMC command line	104	IO	SD2_CMD	-
SD_DETECT	SD/SDIO/MMC card detection (active high)	105	I	SD2_CD_B	PU
SD_D0	SD/SDIO/MMC data line	106	IO	SD2_DATA0	-
SD_D1	SD/SDIO/MMC data line	107	IO	SD2_DATA1	-
SD_D2	SD/SDIO/MMC data line	108	IO	SD2_DATA2	-
SD_D3	SD/SDIO/MMC data line	109	IO	SD2_DATA3	-

Table 49: SD/MMC

8 Onboard components

This chapter describes the onboard components. The used CPU connections are typically not available outside of the DHCOM module.

8.1 eMMC

As non-volatile data storage, the DHCOM i.MX8M Plus module provides an eMMC flash memory to store the operating system and application data on it. It is connected to the 8-bit USDHC3 interface of the i.MX8M Plus SoC. The size of the eMMC starts from 8 GByte and depends on the ordering configuration.

See also Figure 24: SD/MMC Interfaces.

Note: eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly.

Please have a look at: https://en.wikipedia.org/wiki/Flash_memory#Write_endurance

Description	IO Type	CPU ball name
eMMC bus clock	O	NAND_WE_B
eMMC command line	O	NAND_WP_B
eMMC data line 0	IO	NAND_DATA04
eMMC data line 1	IO	NAND_DATA05
eMMC data line 2	IO	NAND_DATA05
eMMC data line 3	IO	NAND_DATA05
eMMC data line 4	IO	NAND_RE_B
eMMC data line 5	IO	NAND_CE2_B
eMMC data line 6	IO	NAND_CE3_B
eMMC data line 7	IO	NAND_CLE
eMMC reset	O	NAND_READY_B

Table 50: eMMC

8.2 LPDDR4

The DHCOM i.MX8M Plus module provides LPDDR4 DRAM. The memory is connected with 32 bit bus width and may be clocked up to 2 GHz. The LPDDR4 memory size can be between 1 Gbyte and 8 Gbyte and depends on the ordering configuration.

The i.MX8M Plus SoC inline ECC for the external LPDDR4 DRAM adds additional safety for high industrial system reliability.

8.3 SPI boot flash

The DHCOM i.MX8M Plus module provides a 16 Mbyte Quad SPI NOR boot flash. By default, the boot mode is set to serial NOR boot and the flash memory contains a preprogrammed standard bootloader.
After power on the i.MX8M Plus ROM code starts up and loads the bootloader from the Quad SPI NOR flash. The bootloader can afterwards start the operating system from other flash devices like eMMC or SD card.
The size of 16 Mbyte offers also the possibility to store a Linux rescue system in the SPI boot flash. This system can be used to install an initial Linux image or to try to rescue the board.
DH electronics recommends the SWUpdate software update for embedded systems. Please have a look at:
https://sbabic.github.io/swupdate/swupdate.html
https://sbabic.github.io/swupdate/scenarios.html

Description	IO Type	CPU ball name
Slave select signal	O	NAND_CE0_B
SPI clock line	O	NAND_ALE
Quad SPI IO0	IO	NAND_DATA00
Quad SPI IO1	IO	NAND_DATA01
Quad SPI IO2	IO	NAND_DATA02
Quad SPI IO3	IO	NAND_DATA03

Table 51: Quad SPI NOR flash

8.4 Wi-Fi® / Bluetooth

The DHCOM i.MX8M Plus module is available with the optional onboard Wi-Fi® and Bluetooth module Type 2AE from muRata. Wi-Fi® is connected to the 4-bit USDHC1 interface of the i.MX8M Plus SoC and Bluetooth® to UART2.
The muRata 2AE uses the Infineon CYW4373E chipset and offers dual band 2.4GHz & 5GHz Wi-Fi® and Bluetooth® 5.2 support. Next to this, the module is FCC/IC and MIC (Japan) "Reference" certified and also the ETSI report is available.

8.4.1 Features

Wi-Fi®:

- Wi-Fi® 802.11a/b/g/n/ac
- Data rate on Wi-fi® PHY up to 433Mbps
- Dual band (2.4 and 5 GHz) support
- Network topology: AP and STA dual mode

Bluetooth®:

- Bluetooth® 5.2 BR/EDR/LE
- Data rate on Bluetooth® PHY up to 3Mbps

8.4.2 Used i.MX8M Plus CPU signals

See also Figure 24: SD/MMC Interfaces.

Notes:

- The DHCOM i.MX8M Plus module is available with chip antenna (option [-WBTA]) on the SoM and additionally also with U.FL connector (option [-WBT]).

Description	IO Type	CPU ball name
SDIO bus clock	O	SD1_CLK
SDIO command line	O	SD1_CMD
SDIO data line 0	IO	SD1_DATA0
SDIO data line 1	IO	SD1_DATA1
SDIO data line 2	IO	SD1_DATA2
SDIO data line 3	IO	SD1_DATA3
WL_REG_EN	O	- (I2C: 0x74; P0.1)

Table 52: SDIO for Wi-Fi®

Description	IO Type	CPU ball name
UART clear to send	I	SD1_DATA5
UART request to send	O	SD1_DATA4
UART receive data line	I	UART2_RXD
UART transmit data line	O	UART2_TXD
BT_REG_EN	O	- (I2C: 0x74; P0.0)
BT_HOST_WAKE	I	- (I2C: 0x74; P1.4)
BT_DEV_WAKE	O	- (I2C: 0x74; P1.5)

Table 53: UART for Bluetooth®

8.5 RTC

The DHCOM i.MX8M Plus module is available with the optional onboard temperature compensated RTC RV-3032-C7 from Micro Crystal. The RTC is connected to the i.MX8M Plus I2C3 port. Please also have a look at chapter 7.9.3 On-module I2CTM.

The RTC can be supplied during time keeping mode via a Goldcap or a button cell battery. Therefore, the supply voltage can be applied through the VCC_BAT SODIMM-200 connection. Please have also a look at 0

Power supply and reset.

Features:

- Factory calibrated temperature compensation
- Very high Time Accuracy (best in class).
  - ±1.5 ppm 0 to +50°C
  - ±3.0 ppm -40 to +85°C
- Low power consumption: 160 nA @ 3 V.
- Wide operating voltage range: 1.3 V to 5.5 V.
- Aging compensation with OFFSET value
- Counters for hundredths of seconds, seconds, minutes, hours, date, month, year and weekday

Notes:

- The INT pin is connected to the IC2 IO Expander: I2C: 0x74; P0.3 (See also 7.9.3 On-module I2CTM)

8.6 EEPROM

8.6.1 EEPROM for ETH 1

The MAC address of the Ethernet 1 controller is stored in the 2 Kbit sized EEPROM (24AA025E48T-I/OT) from Microchip. It is connected to the onboard I2C-Interface (see 7.9.3 On-module I2CTM) and is reachable at the 7 bit address 0x50. It can also be used to store additional data on it. However, only the addresses from 0x00 to 0x80 are user accessible.

The MAC-address itself is stored inside the permanently write protected area of the EEPROM on the addresses 0xFA to 0xFF.

8.6.2 EEPROM for ETH 2

The MAC address of the Ethernet 2 controller is stored in the 2 Kbit sized EEPROM (24AA025E48T-I/OT) from Microchip. It is connected to the onboard I2C-Interface (see 7.9.3 On-module I2CTM) and is reachable at the 7 bit address 0x53. It can also be used to store additional data on it. However, only the addresses from 0x00 to 0x80 are user accessible.

The MAC-address itself is stored inside the permanently write protected area of the EEPROM on the addresses 0xFA to 0xFF.

8.7 microSD socket

The onboard microSD socket is connected to USDHC2 port of the i.MX8M Plus which can be used as a boot source (see 6 Boot Mode). This socket is only populated when ordering the DHCOM i.MX8M Plus with the option [-SD].

The interface supports SDR104 bus speed grade in the UHS-I class. To support this, 1.8V IO voltage switch is needed. The IO voltage of the SDIO power block can be changed independently from the other IO blocks, but all SDIO block signals change their voltages together. The IO voltage for the microSD interface (i.MX 8M Plus USDHC2) is provided by the LDO5 output of the power management IC (PMIC). The voltage level is controlled by the dedicated USDHC2_VSELECT output of the USDHC2 interface.

Notes:

- The microSD interface is shared with the SDIO interface at the SODIMM-200 socket. If option [-SD] is selected, the microSD socket is mounted and the SDIO interface on the SODIMM is not available.

Description	IO Type	CPU ball name
SD bus clock	O	SD2_CLK
SD command line	IO	SD2_CMD
SD card detection (active low)	I	SD2_CD_B
SD data line 0	IO	SD2_DATA0
SD data line 1	IO	SD2_DATA1
SD data line 2	IO	SD2_DATA2
SD data line 3	IO	SD2_DATA3
USDHC2_VSELECT	O	GPIO1_IO04

Table 54:SDIO for the microSD socket

9 Technical specifications

9.1 Operating conditions – Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT	3.3		3.6	V
		4.5		5.5	V
VCC_{ripple} (Vin)	VCC ripple peak-to-peak		50	100	mV
V_{bat}	RTC backup supply voltage	1.2		5.5	V
V_{sysbus}	System bus voltage OUTPUT		3.3		V
$I_{Vsysbus}$	Vsysbus current			20	mA
V_{disp}	Display voltage OUTPUT		1.8		V
I_{Vdisp}	Vdisp current			20	mA
V_{cam}	Camera voltage OUTPUT		3.3		V
I_{Vcam}	Vcam current			20	mA
V_{IO}	I/O voltage OUTPUT		3.3		V
I_{VIO}	VIO current			20	mA
$V_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
$I_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED current			60	mA
IVbat_Stby	RTC timekeeping mode		160	240	nA
VIH_3V3	Digital input high voltage	2.4	3.3	3.5	V
VIL_3V3	Digital input low voltage	-0.3	0	0.8	V

Table 55: DC operating conditions

9.2 Operating conditions – Power examples

Symbol	Description	Min	Typ	Max	Unit
$P_{i.MX8MPlus\_IDLE}$	SOM Power consumption with quad core (1.6 GHz) variant in Idle mode; VCC (Vin) = 3.3 V		1.7		W
	Test condition „IDLE“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) without Display and Ethernet connection. Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz Measured at X43 of PDK2 after system boot and user log in, without any additional scripts. Average power consumption during 60 seconds.				
$P_{i.MX8MPlus\_STRESS-TEST}$	SOM Power consumption with quad core (1.6 GHz) variant, GPU benchmark and CPU stress test; VCC (Vin) = 3.3 V		4.4	5.2	W

	Test condition „STRESS-TEST“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) and additional Display at HDMI port. Average power consumption during 60 seconds.
	Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz
	Measured at X43 of PDK2 after system boot and user log in.
	Test scripts:
	`# XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 glmark2-es2-wayland --off-screen --run-forever >> ~/glmark2-es2-wayland.log &`
	`# XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 weston-simple-egl -f >> ~/weston-simple-egl.log &`
	`# stress-ng -c 4 >> /dev/null &`
	Description:				

Symbol	Description	Min	Typ	Max	Unit
	▪ The first instance of glmark will render into offscreen buffer, without any frame limiting, so the GPU would render as much as it can and consume as much power as it can. ▪ The second instance of weston-simple-egl would only trigger screen redraw, at up to 60 FPS, only to move some memory around and exercise the display pipeline. ▪ stress-ng test runs on all four cores. Average current consumption during 60 seconds.				
$P_{i.MX8MPlus\_STRESS-TEST+NPU}$	SOM Power consumption with quad core (1.6 GHz) variant, GPU benchmark, CPU stress test and NPU benchmark; VCC (Vin) = 3.3 V		7.0	8.0	W

	Test condition „ STRESS-TEST+NPU“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) and additional Display at HDMI port. Average power consumption during 60 seconds.
	Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz
	Measured at X43 of PDK2 after system boot and user log in.
	Test scripts:
	`# XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 glmark2-es2-wayland --off-screen --run-forever >> ~/glmark2-es2-wayland.log &`
	`# XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 weston-simple-egl -f >> ~/weston-simple-egl.log &`
	`# stress-ng -c 4 >> /dev/null &`
	`# cd /usr/bin/tensorflow-lite-2.8.0/examples/`
	`# ./benchmark_model --graph=mobilenet_v1_1.0_224_quant.tflite --external_delegate_path=/usr/lib/libvx_delegate.so --num_runs=5000 --min_secs=800 --max_secs=15000 >> ~/benchmark_model.log &`
	Description:
	▪ The first instance of glmark will render into offscreen buffer, without any frame limiting, so the GPU would render as much as it can and consume as much power as it can.
	▪ The second instance of weston-simple-egl would only trigger screen redraw, at up to 60 FPS, only to move some memory around and exercise the display pipeline.
	▪ stress-ng test runs on all four cores.
	▪ NPU-test: The default number of runs is 50, min_secs is 1 and max_secs is 150 , which runs for about 8-10 seconds. The above would thus run for at least 800 seconds due to min_secs=800 .				

$P_{i.MX8MPlus\_Gbit/s-Eth.}$	SOM Power consumption with quad core (1.6 GHz) variant and iperf3 test on Gbit/s Ethernet port; VCC (Vin) = 3.3 V		3.5	4.3	W

	Test condition „Gbit/s-Eth.“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) and Gbit/s Ethernet port connected to iperf3 server. Average power consumption during 60 seconds.
	Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz
	Measured at X43 of PDK2 after system boot and user log in.
	Test scripts:
	`# ethtool --set-eee ethsom0 eee off`
	`# iperf3 -c 192.168.179.3 -t 1000 >> /dev/null &`
	Description:
	▪ EEE feature disabled and iperf3 test started.				

$P_{i.MX8MPlus\_Gbit/s-Eth.+Wi-Fi}$	SOM Power consumption with quad core (1.6 GHz) variant, iperf3 test on Gbit/s Ethernet port and iperf3 test via Wi-Fi connection; VCC (Vin) = 3.3 V		4.5	5.5	W
	Test condition „Gbit/s-Eth.+Wi-Fi“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) and Gbit/s Ethernet port connected to iperf3 server. Average power consumption during 60 seconds. Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz Measured at X43 of PDK2 after system boot and user log in.				

<table>
<tr><th>Symbol</th><th>Description</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td></td><td colspan="5">Test scripts:
ethtool --set-eee ethsom0 eee off
iperf3 -c 192.168.179.3 -t 1000 >> /dev/null &
ip link set wlansom0 up
wpa_supplicant -i wlansom0 -c /etc/wpa_supplicant.conf >> /dev/null &
iperf3 -c 192.168.117.207 -t 1000 >> /dev/null &
Description:
▪ EEE feature disabled and iperf3 test started.
▪ Connect Wi-Fi interface to Router and start iperf3 test.</td></tr>
<tr><td>P_{i.MX8MPlus_STRESS-TEST+NPU+ Gbit/s-Eth.+Wi-Fi}</td><td>SOM Power consumption with quad core (1.6 GHz) variant, GPU benchmark, CPU stress test, NPU benchmark, Gbit/s Ethernet port iperf3 test and Wi-Fi iperf3 test; VCC (Vin) = 3.3 V</td><td></td><td>9.0</td><td>10.6</td><td>W</td></tr>
<tr><td></td><td colspan="5">Test condition „ STRESS-TEST+NPU+ Gbit/s-Eth.+Wi-Fi“: DHCOM i.MX8M Plus variant HI00104 inside PDK2 (516-400) and additional Display at HDMI port. Average power consumption during 60 seconds.
Image: downstream/imx-image-full-dh-imx8mp-dhcom-pdk2-20221025172940.rootfs.wic.xz
Measured at X43 of PDK2 after system boot and user log in.
Test scripts:
XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 glmark2-es2-wayland --off-screen --run-forever >> ~/glmark2-es2-wayland.log &
XDG_RUNTIME_DIR=/var/run/user/0/ WAYLAND_DISPLAY=wayland-0 weston-simple-egl -f >> ~/weston-simple-egl.log &
stress-ng -c 4 >> /dev/null &
cd /usr/bin/tensorflow-lite-2.8.0/examples/
./benchmark_model --graph=mobilenet_v1_1.0_224_quant.tflite --external_delegate_path=/usr/lib/libvx_delegate.so --num_runs=5000 --min_secs=800 --max_secs=15000 >> ~/benchmark_model.log &
ethtool --set-eee ethsom0 eee off
iperf3 -c 192.168.179.3 -t 1000 >> /dev/null &
ip link set wlansom0 up
wpa_supplicant -i wlansom0 -c /etc/wpa_supplicant.conf >> /dev/null &
iperf3 -c 192.168.117.207 -t 1000 >> /dev/null &
Description:
▪ The first instance of glmark will render into offscreen buffer, without any frame limiting, so the GPU would render as much as it can and consume as much power as it can.
▪ The second instance of weston-simple-egl would only trigger screen redraw, at up to 60 FPS, only to move some memory around and exercise the display pipeline.
▪ stress-ng test runs on all four cores.
▪ NPU-test: The default number of runs is 50, min_secs is 1 and max_secs is 150 , which runs for about 8-10 seconds. The above would thus run for at least
800 seconds due to min_secs=800 .
▪ EEE feature disabled and iperf3 test started.
▪ Connect Wi-Fi interface to Router and start iperf3 test.</td></tr>
</table>

Table 56: Power examples

Notes:

- The typical values of the Power consumption vary between different modules, temperatures, the CPU load as well as external devices connected to the DHCOM module.

9.3 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
RESET_IN	System Reset input assertion time (active low)	10			ms
RESET_OUT	System Reset output assertion time (active low)	10			ms

Table 57: Reset Timings

9.4 Dimensions

Notes:

- Figure 25 shows an example with 5,2mm SODIMM-200 socket height.

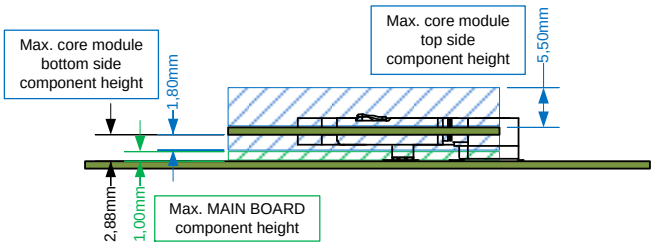

Figure 25: Maximum component heights

9.4.1 Without DHCOM-X connector

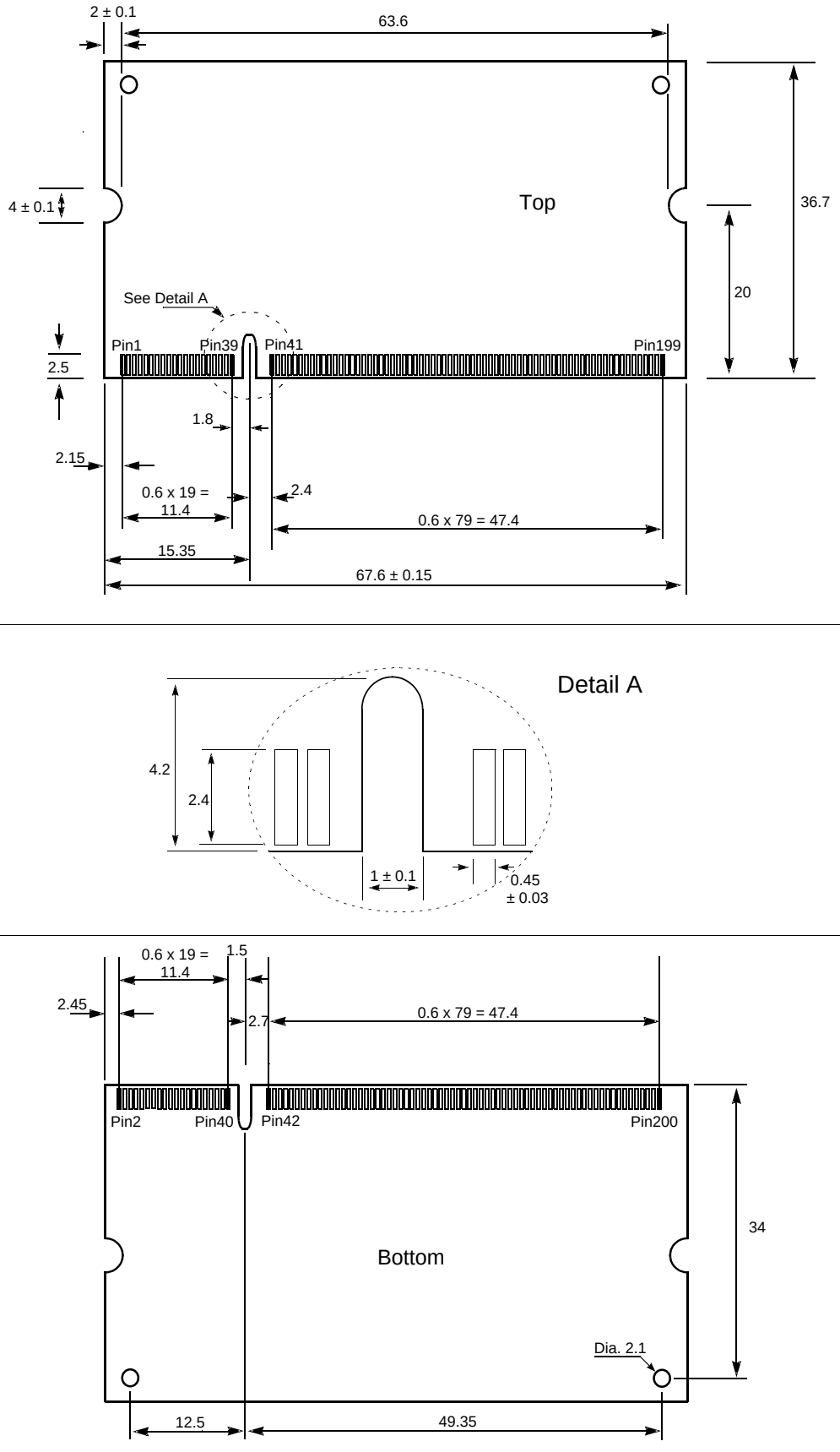

Figure 26: Dimensions of the DHCOM Module without the DHCOM-X connector

9.4.2 With DHCOM-X connector

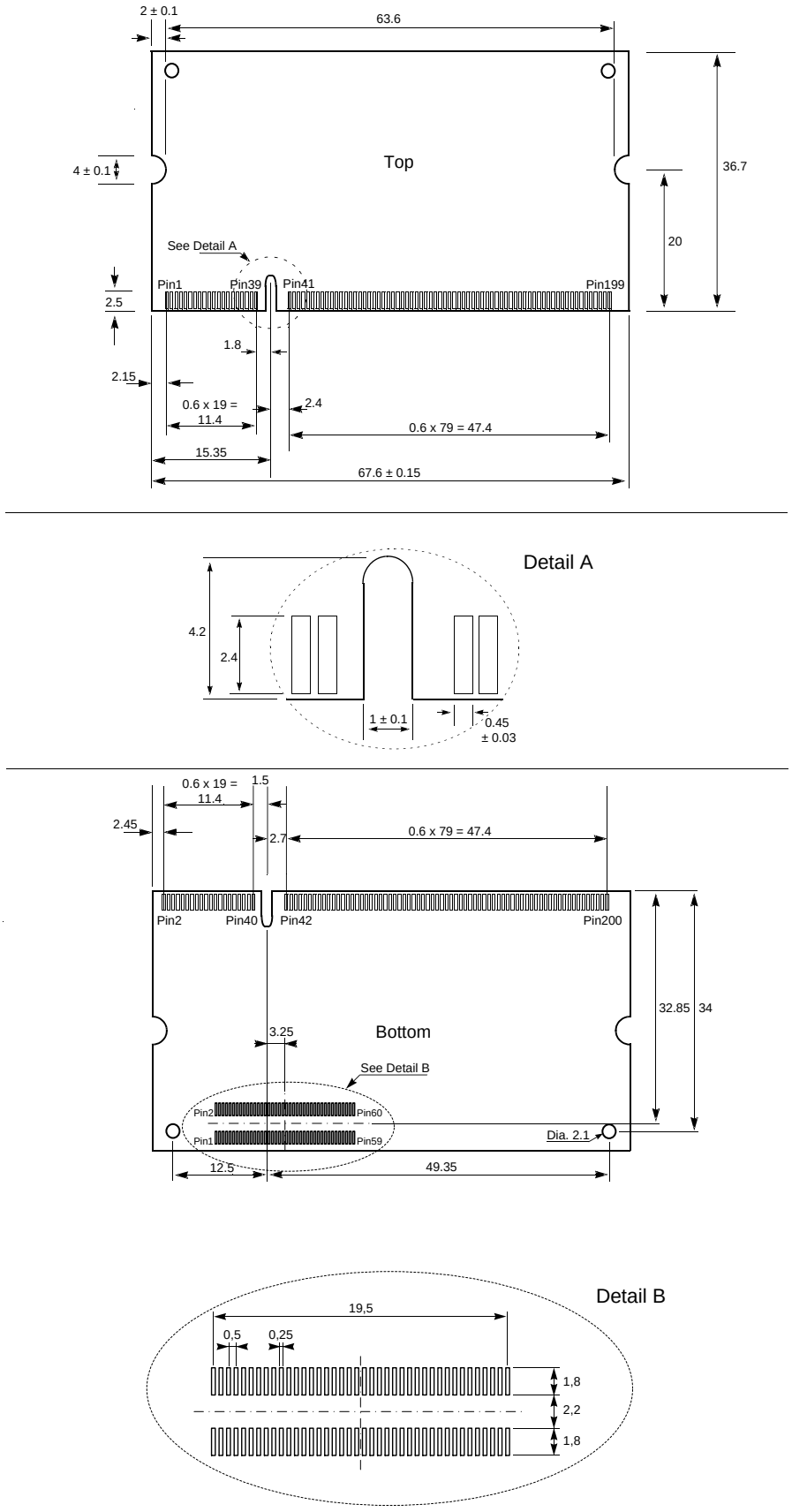

Figure 27: Dimensions of the DHCOM Module with the DHCOM-X connector

9.5 Mechanical system

Several suggestions are given for the plugs, sockets and cables in the following subsections.

9.5.1 SODIMM-200 socket

The DHCOM i.MX8M Plus module is designed for operation in a standard 2.5V (DDR) SODIMM-200 memory socket.
The following sockets have been successfully tested with the module:

Manufacturer	Description	Article number
Tyco Electronics https://www.te.com/	Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm	1473005-1
Nexus Components https://www.nexus-de.com/en	Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm	5214HB52
E-tec Interconnect https://www.e-tec.com/v5/	Plug height: 5.2 mm Max. main board component height below the module: 1.0 mm	DMD-200-RSE9-55
Tyco Electronics https://www.te.com/	Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm	1612618-1
Nexus Components https://www.nexus-de.com/en	Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm	5214HB92
E-tec Interconnect https://www.e-tec.com/v5/	Plug height: 9.2 mm Max. main board component height below the module: 5.0 mm	DMD-200-RPE9-55

Figure 28: SODIMM-200 sockets

9.5.2 DHCOM-X connector

A Molex (https://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector.

DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

SODIMM-200 socket height	Description	Article number
5.2 mm	0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits	Molex 53748-0808
9.2 mm	Not available	Not available

Figure 29: DHCOM-X sockets

9.5.3 JTAG cable

Manufacturer	Description	Article number
Würth Elektronik https://www.we-online.com/	0.50 mm flat flexible cable Type 1 WR-FPC	687 610 050 002
Molex https://www.molex.com/	0.50 mm flat flexible cable Type A	982660097

Figure 30: FFC Cable

9.5.4 JTAG Tag-Connect cable

Manufacturer	Description	Article number
Tag-Connect https://www.tag-connect.com/	10 pin No-Legs Tag-Connect cable	TC2050-IDC-NL

9.6 Temperature range

Symbol	Operating temperature range	Min	Typ	Max	Unit
T_AMB	Standard configuration	-25		85	°C
T_AMB	On request	-40		85	°C

Figure 31: Temperature range

10 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

10.1 i.MX8M Plus processor

Data sheets and technical documents can be found at https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS

10.2 PCA9450CHN power manager

Data sheets and technical documents can be found at https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/power-manage-ic-pmic-for-i-mx-8m-mini-nano-plus:PCA9450

10.3 TSC2014 res. touch controller

Data sheets and technical documents can be found at http://www.ti.com/product/TSC2014

10.4 ADS1015 AD-converter

Data sheets and technical documents can be found at https://www.ti.com/product/ADS1015

10.5 RV-3032-C7 real time clock

Data sheets and technical documents can be found at https://www.microcrystal.com/en/products/real-time-clock-rtc-modules/rv-3032-c7/

10.6 LAN8740Ai ethernet PHY

Data sheets and technical documents can be found at https://www.microchip.com/en-us/product/LAN8740A

10.7 KSZ9131RNXI Gbit ethernet PHY

Data sheets and technical documents can be found at https://www.microchip.com/en-us/product/KSZ9131

10.8 TC9595XBG MIPI® DSI-to-RGB bridge

Data sheets and technical documents can be found at https://toshiba.semicon-storage.com/eu/semiconductor/product/interface-bridge-ics-for-mobile-peripheral-devices/display-interface-bridge-ics/detail.TC9595XBG.html

10.9 2AE Wi-Fi®/Bluetooth module

Data sheets and technical documents can be found at https://www.murata.com/en-eu/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type2ae

11 RoHS conformance

This device has been manufactured RoHS II-compliant.