# User Manual

DHCOM STM32MP1

DH electronics GmbH ▪ Am Anger 8 ▪ 83346 Bergen ▪ Germany

YOUR DIGITAL HEROES.

**History**

| Version | Data | Description of changes | Name |
|---|---|---|---|
| R01 | 08.07.2020 | First version | AG, MH |
| R01 | 13.07.2020 | Reviewed and released (see #7512) | AG, MH |
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# Abbreviations

- AC'97 = Audio Codec '97
- ADC = Analog to Digital Converter
- AIN = Analog input
- AINOUT = Analog input/output
- CAN = Controller Area Network
- CAN FD = CAN Flexible Data Rate
- CMOS = Complementary Metal Oxid Semiconductor
- DAC = Digital to Analog Converter
- DSI = Display Serial Interface
- FMC = Flexible memory controller
- FMC = Flexible Memory Controller
- GPIO = General Purpose Input / Output
- I = Input
- I2C™ = Inter-Integrated Circuit
- I2S = Inter-IC Sound
- IO = Input/output
- ISO = International Organization for Standardization
- JPEG = Joint Photographic Experts Group
- LCD = Liquid Crystal Display
- LTS = Long Term Support
- MBC = Must be connected
- MIPI Alliance = Mobile Industry Processor Interface Alliance
- MLC = Multi-Level Cell
- O = Output
- PCM/DSP = Pulse-Code Modulation/Digital Signal Processing
- PD = Pull-Down
- PHY = Physical Layer
- PMBus = Power Management Bus
- PU = Pull-Up
- PWM = Pulse Width Modulation
- PWR_I = Power input
- PWR_O = Power output
- RGB = Red, green, and blue

- RTC = Real Time Clock
- SAI = Serial Audio Interface
- SMBus = System Management Bus
- SPI = Serial Peripheral Interface
- TBD = To be defined
- TFT = Thin-Film Transistor
- TTCAN = Time Triggered Communication on CAN
- UART = Universal Asynchronous Receiver Transmitter
- YCbCr = Is a family of color spaces. Y is the luma component and CB and CR are the blue-difference and red-difference chroma components.

# 1 Introduction

## 1.1 Hardware

The module from the STM32MP1 family is now available as solderable DHCOR STM32MP1 version and as pluggable DHCOM STM32MP1 module. The module has a long-term availability of 10+ years and fits perfectly into the DH family concept with its SODIMM-200 socket. It is a powerful heterogeneous SoC with ARM® Dual Cortex-A7 @800 MHz and ARM® Cortex-M4 @209 MHz.

On the STM32MP1 there are many embedded interfaces like two 16 bit ADCs, 12 bit DACs, PWM/Timer, GPIO, UART, SPI, RTC, up to 2x FD-CAN and standard features like I2S, I2C™, two 100 Mbit Ethernet ports with PHY, 8 or 10 bit camera interface, SD/MMC and one USB 2.0 High Speed OTG and host port each. Furthermore, a parallel 16 bit bus interface is available, which can be used e.g. to connect an FPGA. A 24 bit RGB or Mipi-DSI connector with HD resolution (1366 x 768 pixels) serves as display interface. The optionally integrated Vivante 3D GPU runs with up to 533 MHz clock frequency, supports Open GL ES 2.0. and enables powerful graphical user interfaces.

The module also features a 32 bit DDR3 connection with a maximum memory expansion of 1 Gbyte. A 2 Mbyte SPI boot Flash and a 4, 8 or 16 Gbyte eMMC Flash are used as flash memory. A 4-wire resistive touch interface is also available. The DHCOM STM32MP1 also features dual-band WiFi IEEE802.11 a/b/g/n and dual-mode Bluetooth 5 with PCB antenna and U.FL connector.

The DHCOM STM32MP1 is suitable for many fields of application and stands out from the crowd with its diverse analogue and digital possibilities. Thus, the STM32MP1 microprocessors enable powerful IoT and/or HMI applications from sensors and actuators to the cloud with only one chip.

**Applications:**

- Industrial Automation
- Machine controls and operator panels (HMI)
- Home & Building
- Medical Technology

## 1.2 Software

The DHCM-STM32MP1-01D2 uses Linux as operating system, which can be based on the Debian distribution or created with Yocto Project.

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.
The DHCM-STM32MP1-01D2 is the first module from the DHCOM family which is from the beginning on up streamed at the Linux mainline Kernel and also in U-Boot. Therefore, the user has the opportunity to switch very easy to the newest available Linux kernel release. The specific vendor-based support of DH electronics is in that case always based on an LTS kernel version.
All available sources are available via Github: https://github.com/dh-electronics
Please also have a look at our Wiki: https://wiki.dh-electronics.com/index.php/Main_Page

## 1.3 Main features

- Dual ARM Cortex®-A7 up to 800 MHz and Single ARM Cortex®-M4 up to 209 MHz
- 3D GPU OpenGL® ES2.0 up to 533 MHz, Power Management: STPMIC1A
- TrustZone, cryptography, hash, secure boot
- DDR3L: 256 / 512 / 1024 Mbyte (32 bit)
- eMMC flash: 4 / 8 / 16 Gbyte
- SPI boot flash: 2 Mbyte
- EEPROM: 256 byte
- WiFi / Bluetooth: WiFi IEEE 802.11 a / b / g / n, 802.11j (hosted mode) with dual band, Bluetooth® v5.0 (BR/EDR/BLE), PCB antenna and U.FL antenna connector
- On-board microSD card socket with support for SDR 104
- RTC with temperature compensation ± 3.0 ppm between -40 to +85°C
- Supply voltage range: 3.3 or 5.0 VDC / typ. 1 W-1.5 W (without WiFi/BT)
- Industrial temperature range: -40°C to +85°C
- SODIMM-200 socket with DHCOM pin assignment
- JTAG debug connection via FFC connector or Tag-Connect
- Bus interface: 16 bit asynchronous address / data bus, 1 CS
- Ethernet 1: 10 / 100 Mbit with PHY, IEEE 1588v2
- Ethernet 2: 10 / 100 Mbit with PHY
- MMC/SD interface: 4 bit mode
- CAN 1: V2.0B and CAN FD V1.0, TTCAN (time triggered)
- CAN 2: V2.0B and CAN FD V1.0
- UART 1: Rx / Tx / Rts / Cts, up to 12.5 Mbit/s
- UART 2: Rx / Tx / Rts / Cts, up to 12.5 Mbit/s
- UART 3: Rx / Tx, up to 12.5 Mbit/s

- SPI 1: max. 50 Mbit/s
- I2C™ 1: max. 1 Mbit/s
- I2C™ 2: max. 1 Mbit/s
- USB host 1: High-Speed
- USB OTG: High-Speed
- Parallel camera: 10 bit interface up to 140 Mbytes/s
- Display RGB: Max. 1366 x 768 pixels, 24 bit
- MIPI®-DSI 2 data lanes up to 1 GHz each
- Touch: 4-wire
- I²S Audio interface
- GPIOs: 24 IOs
- PWM: 1x 16 bit
- Analog: 4x 16 bit ADC and 2x 12 bit DAC

## 1.4 Further technical information

For more precise technical information, we refer you to the websites of the chip manufacturers:

### 1.4.1 STM32MP1 processor

Data sheets and technical documents can be found at https://www.st.com/en/microcontrollers-microprocessors/stm32mp1-series.html

### 1.4.2 STPMIC1A power manager

Data sheets and technical documents can be found at https://www.st.com/en/power-management/stpmic1.html

### 1.4.3 TSC2014 res. touch controller

Data sheets and technical documents can be found at http://www.ti.com/product/TSC2014

### 1.4.4 RV-8803-C7 real time clock

Data sheets and technical documents can be found at https://www.microcrystal.com/en/products/real-time-clock-rtc/rv-8803-c7/

### 1.4.5 LAN8710Ai ethernet PHY

Data sheets and technical documents can be found at https://www.microchip.com/wwwproducts/en/LAN8710A

### 1.4.6 KSZ8851-16MLLI ethernet controller

Data sheets and technical documents can be found at https://www.microchip.com/wwwproducts/en/KSZ8851

### 1.4.7 RS9116N-DB00-CC1 WiFi/Bluetooth module

Data sheets and technical documents can be found at

https://www.redpinesignals.com/Products/Hosted_Connectivity/Multi-Protocol_Wireless_SoCs_&_Modules/RS9116_SoCs_&_Modules/RS9116N-DB00-CC1.php

# 2 Hardware overview

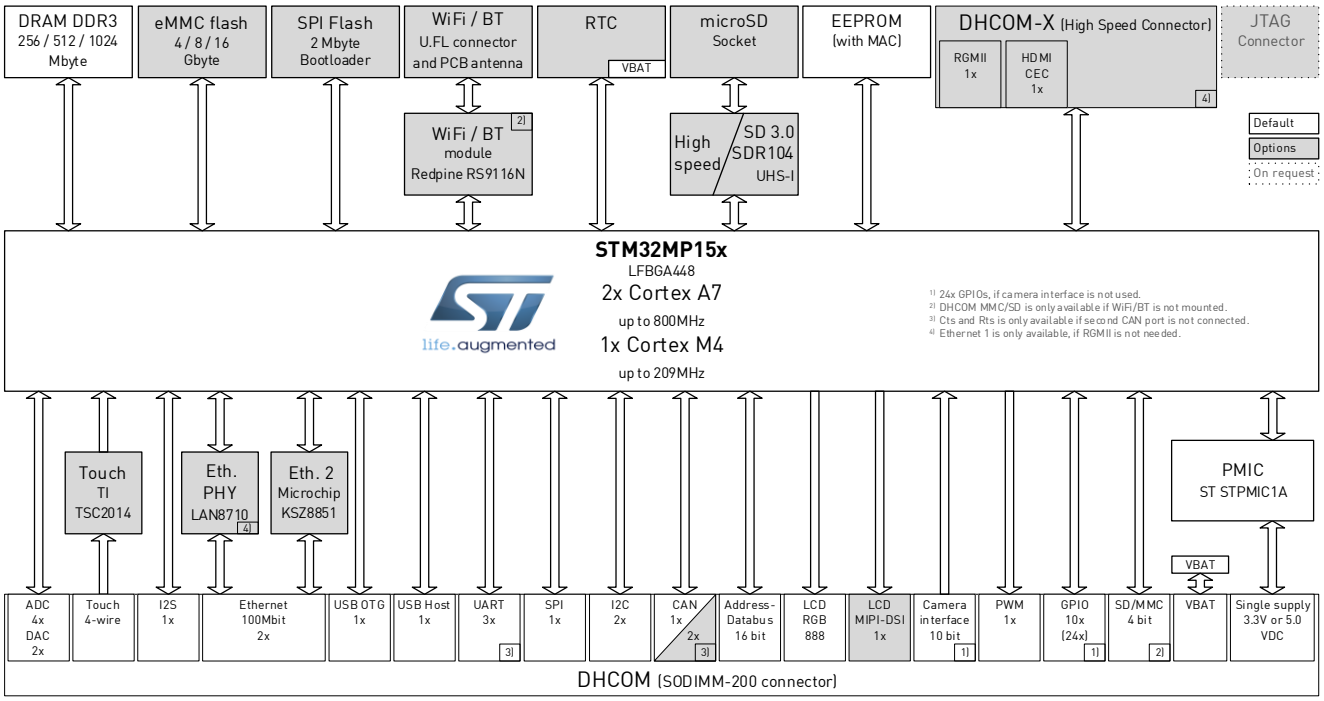


*Figure 1: DHCM-STM32MP1-01D2 block diagram*

# 3 DHCOM hardware compatibility

The following subsections describe the signals at the SODIMM-200 socket.

**Notes:**

- For all specified pull-up and pull-down resistors, a value of 10k is recommended.
- "Not used" specification describes, what needs to be done with unconnected pins.

The DHCOM specification specifies function groups in order to ensure compatibility between various DHCOM modules. Each function group has its own voltage level output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters on the customer specific main board provide compatibility between various DHCOM modules. Naturally, these level shifters can also be removed from the customer design. In this case, the customer will lose compatibility to the DHCOM standard.

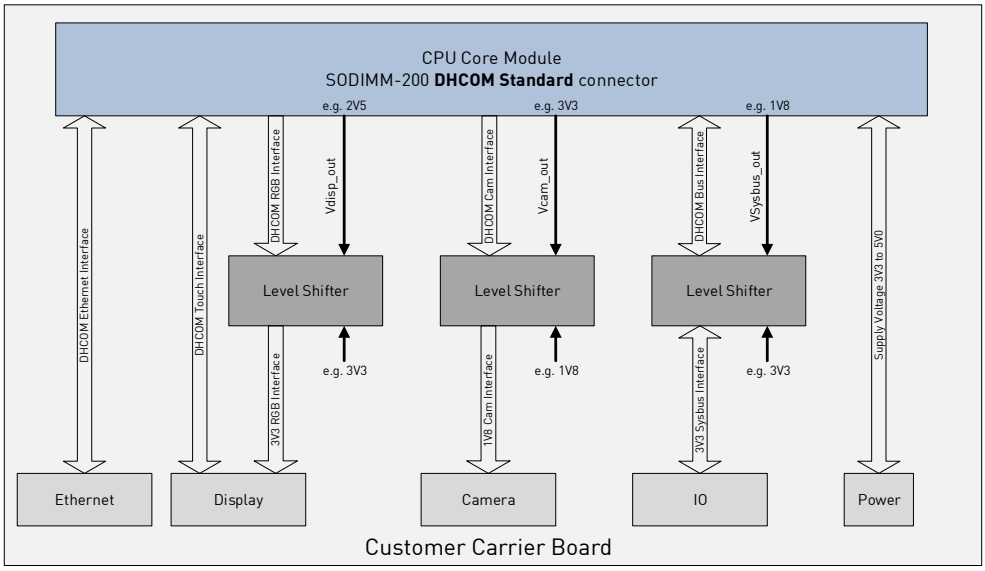


*Figure 2: DHCOM functions groups concept*

**Important:**

With the level shifter concept, it is possible to support all core modules which are developed from DH electronics in the future. If you only like to use the current DHCOM modules (DHCOM i.MX25, i.MX6ULL, i.MX6 and AM335x) you only need to use level shifters in special cases, if you have a look at the following table:

| Voltage | i.MX25 | i.MX6UL(L) | AM335x | STM32MP1 | i.MX6 |
|---|---|---|---|---|---|
| **VCC (Vin)** | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V | 3.3V – 5.5V |
| **$V_{BAT}$** | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V | 1.3V – 4.0V |
| **$V_{SYSBUS}$** | 1.8V | Not available (3.3V) | Not available (3.3V) | 3.3V | 3.3V |
| **$V_{DISP}$** | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V |
| **$V_{CAM}$** | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V |
| **$V_{IO}$** | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V |
| **$V_{ETH\_VIO\_SWITCHED}$** | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V |
| **USB_OTG_VBUS** | 5.0V | 5.0V | 5.0V | 5.0V | 5.0V |

*Table 1: Voltage groups*

# 4 Power supply and reset

### 4.1.1 Power supply

The DHCM-STM32MP1-01D2 has the following power connections:

- Vin = Core module supply voltage input
- $V_{BAT}$ = Battery voltage input
- $V_{SYSBUS}$ = System bus voltage output
- $V_{DISP}$ = Display voltage output
- $V_{CAM}$ = Camera voltage output
- $V_{IO}$ = I/O voltage output

**Notes to $V_{BAT}$:**

- When no buffer battery is used in the system, $V_{BAT}$ must be connected to 3.3V.
- When ordering a DHCOM STM32MP1 without the option [-RTC], $V_{BAT}$ is connected to the internal RTC of the STM32MP1.
- In applications, where a long buffer of date and time is needed, we recommend the option [-RTC], which uses the RV-8803-C7 instead of the internal RTC. This external RTC supports temperature compensation which leads to a higher accuracy, while at the same time it is running with a lower power consumption, than the internal RTC. When ordering the DHCOM STM32MP1 with the option [-RTC], $V_{BAT}$ is connected to the RV-8803-C7 only. For more information about this option have a look at chapter 8.5 "RTC".

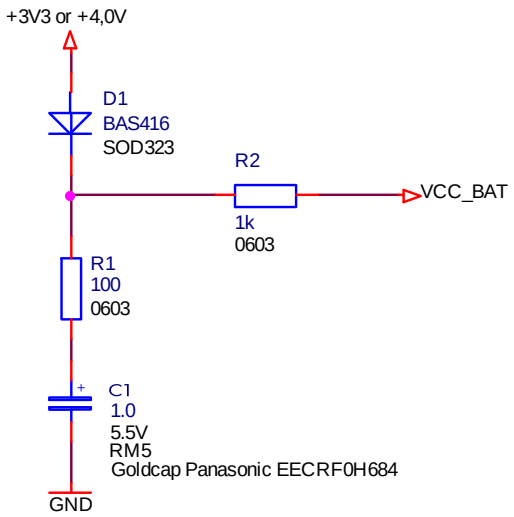


*Figure 3: Vbat GoldCap example*

The power supply connections Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT are to be used to detect the correct voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with the level shifter.

### 4.1.2 Reset signals

The System is put in reset state by holding RESET_IN signal low.
When the RESET_IN is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_OUT is asserted as long as RESET_IN is asserted. If the reset input RESET_IN is de-asserted, the RESET_OUT is also de-asserted and the module starts booting again.

### 4.1.3 Pin Reset Status

After a reset, all STM32MP1 GPIOs are in analog mode to reduce power consumption. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.
For each GPIO the following I/O configuration can be set:

- Input mode
- General purpose output mode
- Alternate function mode
- Analog mode

Note: Refer to GPIO port mode register (GPIOx_MODER) for detailed information. (RM0436 "STM32MP157 Reference manual")

### 4.1.4 Signal Overview

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| VCC_IN1 | Core Module supply voltage input | 38 | PWR_I | - | MBC |
| VCC_IN2 | Core Module supply voltage input | 39 | PWR_I | - | MBC |
| VCC_IN3 | Core Module supply voltage input | 40 | PWR_I | - | MBC |
| VCC_IN4 | Core Module supply voltage input | 41 | PWR_I | - | MBC |
| VCC_IN5 | Core Module supply voltage input | 42 | PWR_I | - | MBC |
| VCC_IN6 | Core Module supply voltage input | 44 | PWR_I | - | MBC |
| GND1 | Core Module Ground | 17 | PWR_I | - | MBC |
| GND2 | Core Module Ground | 19 | PWR_I | - | MBC |
| GND3 | Core Module Ground | 43 | PWR_I | - | MBC |
| GND4 | Core Module Ground | 45 | PWR_I | - | MBC |
| GND5 | Core Module Ground | 47 | PWR_I | - | MBC |
| GND6 | Core Module Ground | 101 | PWR_I | - | MBC |
| GND7 | Core Module Ground | 111 | PWR_I | - | MBC |
| GND8 | Core Module Ground | 153 | PWR_I | - | MBC |
| GND9 | Core Module Ground | 185 | PWR_I | - | MBC |
| GND10 | Core Module Ground | 199 | PWR_I | - | MBC |
| VCC_BAT | Core Module Battery voltage input | 200 | PWR_I | - | MBC |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| VDDA_Audio | Audio Codec supply voltage input<br>(Not connected on the DHCOM STM32MP1, because the DHCOM STM32MP1 module is not available with onboard Audio Codec) | 10 | PWR_I | - | MBC |
| VSSA_Audio | Audio Codec Ground | 9 | PWR_I | - | MBC |
| Vsysbus_OUT | System bus supply voltage output | 110 | PWR_O | - | - |
| Vdisp_OUT | LCD controller supply voltage output | 46 | PWR_O | - | - |
| Vcam_OUT | Camera supply voltage output | 102 | PWR_O | - | - |
| VIO_OUT | I/O supply voltage output | 152 | PWR_O | - | - |
| RESET_IN | System Reset input (active low) | 21 | I | - | - |
| RESET_OUT | System Reset output (active low) | 20 | O | - | - |

*Table 2: SODIMM-200 Power supply and reset*

**Notes:**

- Since on the DHCOM STM32MP1 VDDA_Audio is not used, it also can be left unconnected. However, in order to support all our DHCOM modules, it is recommended to connect it. (See 3 DHCOM hardware compatibility)

# 5 Hardware coding

The following pins can be used to identify the current hardware version of the DHCOM STM32MP1 module.

| CPU ball name | Description | IO Type |
|---|---|---|
| PF12 | Code_HW_0 | I |
| PF13 | Code_HW_1 | I |
| PF15 | Code_HW_2 | I |

*Table 3: Hardware coding*

| DH PCB number | Description | Code_HW_2 | Code_HW_1 | Code_HW_0 |
|---|---|---|---|---|
| 587-100 (current version) | DHCM-STM32MP1-01D2 HW100 | 0 (10k PD) | 0 (10k PD) | 0 (10k PD) |
| ... | ... | 0 (10k PD) | 0 (10k PD) | 1 (10k PU) |
| | | 0 (10k PD) | 1 (10k PU) | 0 (10k PD) |
| | | 0 (10k PD) | 1 (10k PU) | 1 (10k PU) |
| | | 1 (10k PU) | 0 (10k PD) | 0 (10k PD) |

*Table 4: PCB versions*

# 6 Boot Mode

During startup the STM32MP1 reads out the BOOT-Pins to select a specific boot mode.

| BOOT2 | BOOT1 | BOOT0 | Initial boot mode | Comment |
|---|---|---|---|---|
| 0 | 0 | 0 | UART and USB | Wait for incoming connection on:<br>-USART2/3/6 and UART 4/5/7/8<br>-USB Host |
| 0 | 0 | 1 | Serial NOR Flash | On-board SPI boot flash |
| 0 | 1 | 0 | eMMC | On-board eMMC |
| 0 | 1 | 1 | ~~NAND Flash~~ | This mode is not available on the DHCOM STM32MP1 |
| 1 | 0 | 0 | Reserved (NoBoot) | Used to get debug access without boot from Flash memory |
| 1 | 0 | 1 | SD card | On-board SD card on SDMMC1 Interface |
| 1 | 1 | 0 | UART and USB | Wait for incoming connection on:<br>-USART2/3/6 and UART 4/5/7/8<br>-USB OTG |
| 1 | 1 | 1 | ~~Serial NAND Flash~~ | This mode is not available on the DHCOM STM32MP1 |

*Table 5: Combination of the BOOT-Pins to select a boot mode*

On the DHCOM STM32MP1 the boot modes are selected by the resistors R244 to R249. As a default, they are set to Serial NOR Flash, to start up from the on-board SPI boot flash, which contains a preprogrammed bootloader. The bootloader can afterwards start the operating system from other flash devices like eMMC or SD card.

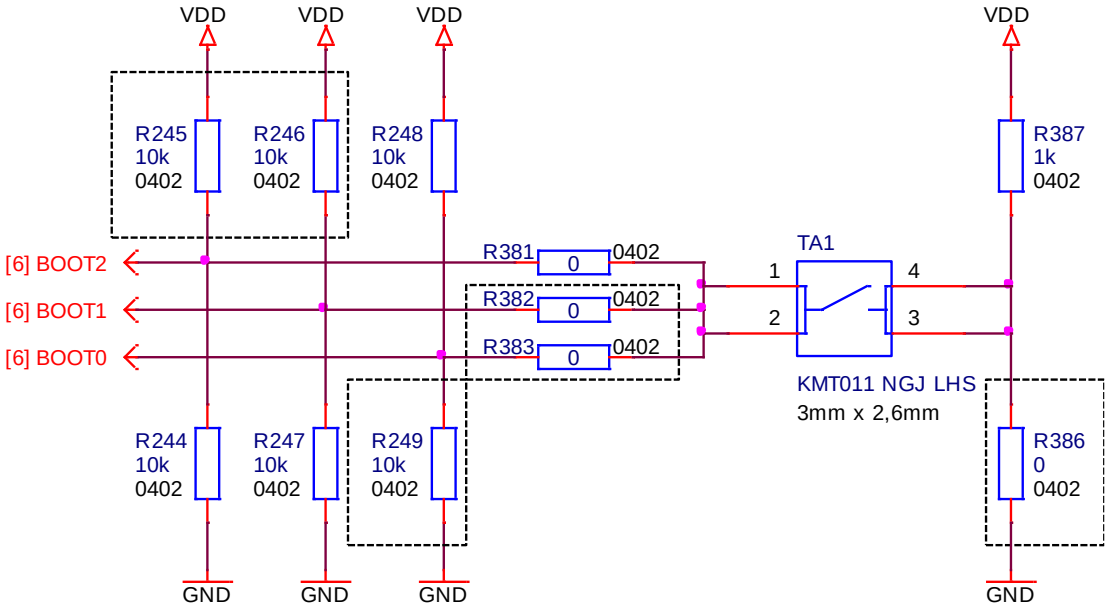


*Figure 4: Selection of the boot mods with push-button to switch to a different mode temporarily*

In Addition to that, the DHCOM STM32MP1 contains a push-button which can be used to override one of the boot-pins temporarily. For instance, the boot-mode can be switched from Serial NOR Flash to SD card by holding down the button during the first seconds of boot-up. However, this button is meant for development use only and therefore it is not populated when it comes to the mass production.
Alternatively, the push-button can be connected to other BOOT-Pins too, by placing a zero-ohm resistor on to the pads of R381, R382 or R383.

- R381 for BOOT2
- R382 for BOOT1
- R283 for BOOT0

The polarity of the push-button can be selected by populating either R386 or R387.

- R386 for LOW
- R387 for HIGH

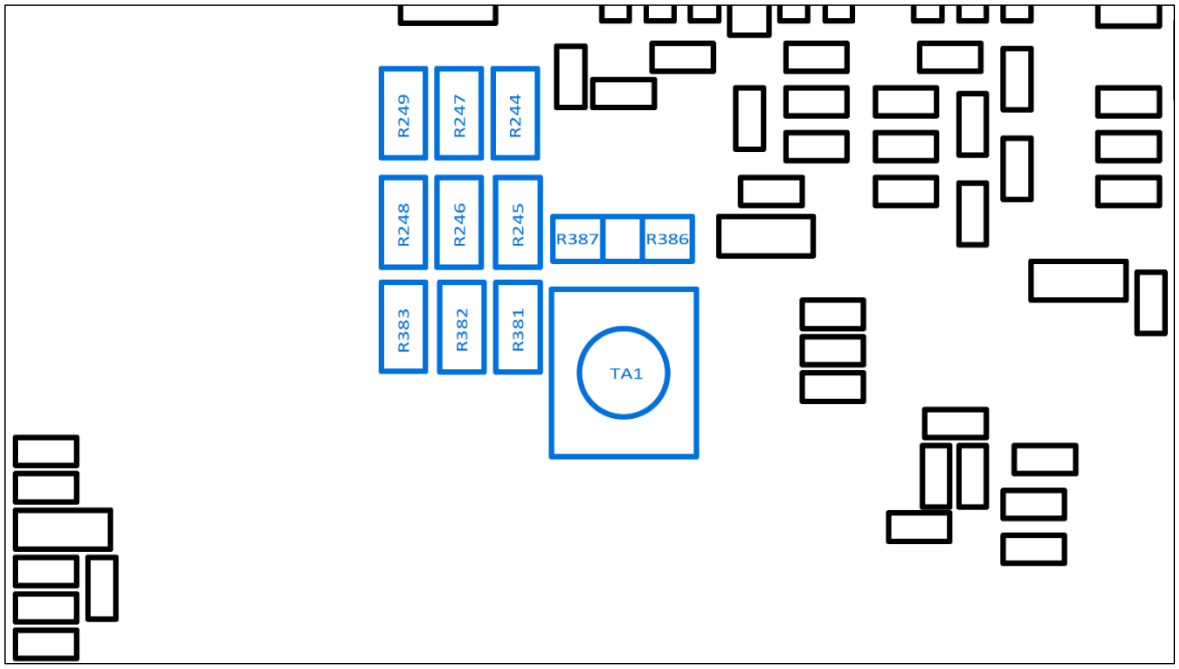


*Figure 5: Assembly of the components related to the BOOT configuration on the topside of the DHCOM STM32MP1*

# 7 Interface description

## 7.1 Ethernet

The DHCOM STM32MP1 module provides two Ethernet interfaces with up to 100BASE-TX full duplex.

For use-cases which might require a Gigabit-Ethernet connection, the Module can be ordered without the on-board Ethernet PHY and the DHCOM-X connector instead (option [-HS]). This connector make access to the RGMII interface of the STM32MP1 on which a Gigabit Ethernet PHY can be connected externally.

If required, the second 100Mbit Ethernet port is still available and the controller can be mounted in addition to the DHCOM-X connector in a customer specific variant.

**Notes:**

- The LED outputs "nETH*_LINK_LED" and "nETH*_SPEED_LED" must be connected as follows:

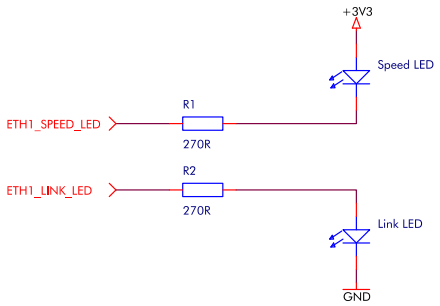


*Table 6: Ethernet LED circuitry*

- In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration straps.
- A special feature of the DHCOM Ethernet interface is the voltage output ETH_VIO_SWITCHED. This output can be used to supply the Ethernet transmitter. In case of low power modes, the output is disabled from the software to save power.

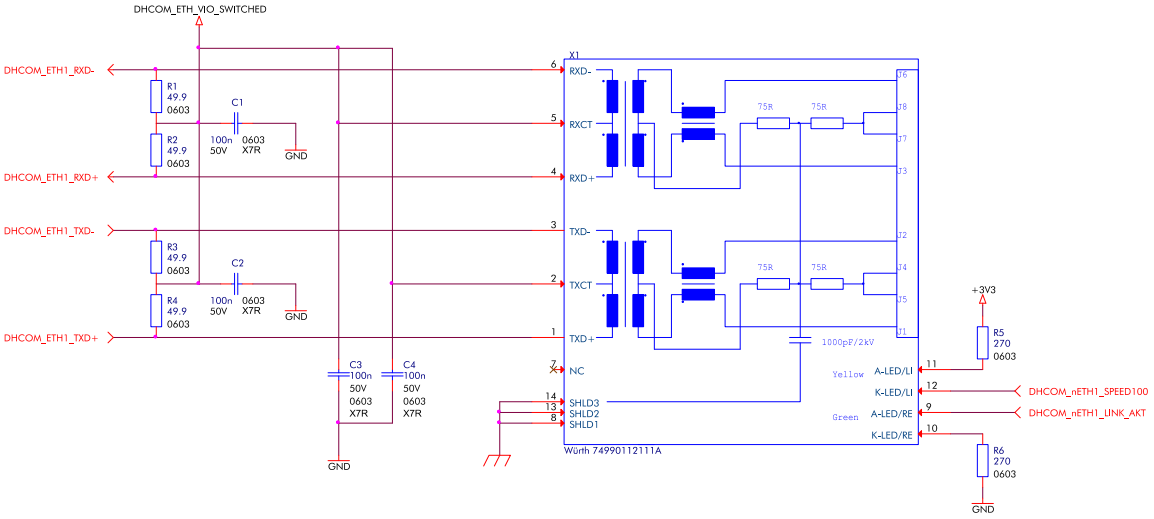


*Figure 6: ETH_VIO_SWITCHED example*

### 7.1.1 ETH1

The Ethernet MAC interface of the STM32MP1 CPU is connected via RMII mode to the PHY LAN8710Ai from Microchip. The PHY address is set to 0x1.

The needed 50MHz clock is provided by the STM32MP1 MCO2 output via PG2 pad of the STM32MP1. The clock is transferred back to the CPU PA1 pad and is internal used as 50MHz reference for the MAC interface.

The STM32MP1 is also connected via I2C™ to a separate EEPROM which contains a MAC address for the ETH1 interface. The I2C™ address of the EEPROM is 0x50. (see also 7.8.3 Onboard I2C and)

The Ethernet interface fulfil the IEEE1588 conform standard.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| nETH1_LINK_LED | Port 1: Activity LED connection | 186 | O | - | PD |
| nETH1_SPEED_LED | Port 1: Speed LED connection | 188 | O | - | PU |
| ETH1_TXD- | Port 1: Ethernet TX Differential Output (minus) | 190 | O | - | PD |
| ETH1_TXD+ | Port 1: Ethernet TX Differential Output (plus) | 192 | O | - | PD |
| ETH_VIO_SWITCHED | Analogue power supply output to magnetics | 194 | PWR_O | - | - |
| ETH1_RXI- | Port 1: Ethernet TX Differential Input (minus) | 196 | I | - | PD |
| ETH1_RXI+ | Port 1: Ethernet TX Differential Input (plus) | 198 | I | - | PD |

*Table 7: Ethernet 1 Connection*

### 7.1.2 ETH2

The STM32MP1 FMC interface (used in multiplexed asynchronous mode) is connected to the Ethernet controller KSZ8851-16MLLI from Microchip.

The Ethernet controller is also connected to a separate EEPROM which contains a MAC address for the ETH2 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| nETH2_LINK_LED | Port 2: Activity LED connection | 187 | O | - | PD |
| nETH2_SPEED_LED | Port 2: Speed LED connection | 189 | O | - | PU |
| ETH2_TXD- | Port 2: Ethernet TX Differential Output (minus) | 191 | O | - | PD |
| ETH2_TXD+ | Port 2: Ethernet TX Differential Output (plus) | 193 | O | - | PD |
| ETH_VIO_SWITCHED | Analogue power supply output to magnetics | 194 | PWR_O | - | - |
| ETH2_RXI- | Port 2: Ethernet TX Differential Input (minus) | 195 | I | - | PD |
| ETH2_RXI+ | Port 2: Ethernet TX Differential Input (plus) | 197 | I | - | PD |

*Table 8: Ethernet 2 Connection*

### 7.1.3 RGMII

Like mentioned in the beginning of this chapter, the RGMII interface is only available when ordering an DHCOM STM32MP1 with the option [-HS]. In that case, ETH1 is not available.

The RGMII interface is available on the additional DHCOM-X connector of the DHCOM module.

| DHCOM-X pin name | Description | DHCOM-X pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| RGMII_RXCLK | Receive Reference Clock | 1 | I | PA1 | - |

| DHCOM-X pin name | Description | DHCOM-X pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| RGMII_RXD0 | Receive Data 0 | 3 | I | PC4 | - |
| RGMII_RXD1 | Receive Data 1 | 5 | I | PC5 | - |
| RGMII_RXD2 | Receive Data 2 | 7 | I | PH6 | - |
| RGMII_RXD3 | Receive Data 3 | 9 | I | PB1 | - |
| RGMII_RX_CTL | Receive Control | 11 | O | PA7 | - |
| RGMII_MDIO | Management Data Input / Output | 13 | IO | PA2 | - |
| RGMII_RST | Ethernet Reset | 15 | O | PH3 | - |
| RGMII_TXCLK | Transmit Reference Clock | 2 | O | PG4 | - |
| RGMII_TXD0 | Transmit Data 0 | 4 | O | PG13 | - |
| RGMII_TXD1 | Transmit Data 1 | 6 | O | PG14 | - |
| RGMII_TXD2 | Transmit Data 2 | 8 | O | PC2 | - |
| RGMII_TXD3 | Transmit Data 3 | 10 | O | PE2 | - |
| RGMII_TX_CTL | Transmit Control | 12 | O | PB11 | - |
| RGMII_MDC | Management Data Clock | 14 | O | PC1 | - |
| RGMII_REFCLK | 125 MHz Clock | 16 | I | PG5 | PU |
| RGMII_INT | Interrupt | 18 | I | PI11 | PU |
| VCC_RGMII_OUT | Power Supply (3V3) | 20 | PWR_O | - | - |

*Table 9: RGMII Interface Connection*

# 7.2 USB

The DHCOM STM32MP1 modules provides both USB 2.0 high-speed Phys of the STM32MP1 to the SODIMM connector. One of these ports supports host mode only, while the second port supports both, host mode and USB OTG.

## 7.2.1 USB OTG

This USB interface fulfils the USB 2.0 specification. It can be configured as OTG, host or device and supports all speed grades at low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) and high-speed (480Mbps).

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| USB_OTG_VBUS | OTG Client: VBUS Input line<br>OTG Host: USB bus supply voltage (reference input) | 166 | I | OTG_VBUS | PD |
| USB_OTG_ID | OTG ID Pin: Connected to the OTG AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client) | 168 | I | PA10 | - |
| USB_OTG_D+ | USB OTG differential Signal positive line | 170 | IO | USB_DP2 | PD |
| USB_OTG_D- | USB OTG differential Signal negative line | 172 | IO | USB_DM2 | PD |

*Table 10: USB OTG*

**Notes:**

- The STM32MP1 PMIC cannot provide the VBUS supply voltage, because this is not compliant with the DHCOM specification.

- The DHCOM USB OTG port does not provide any "enable" and "over current" signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event, the "over current" output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

### 7.2.2 USB Host

The DHCOM STM32MP1 module provides an USB 2.0 compliant host interface, supporting data transfers at low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) and high-speed (480Mbps).

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| USB_PWR_STAT | USB Host over current indicator (active low) | 174 | I | PA14 | - |
| USB_PWR_EN | USB Host power enable signal (active low) | 176 | O | PA13 | - |
| USB_HOST_D1+ | USB Host differential Signal positive line | 178 | IO | USB_DP1 | PD |
| USB_HOST_D1- | USB Host differential Signal negative line | 180 | IO | USB_DM1 | PD |

*Table 11: USB Host*

**Note:** The STM32MP1 PMIC cannot provide the VBUS supply voltage, because this is not compliant with the DHCOM specification.

## 7.3 ADC / DAC

The DHCOM STM32MP1 module provides 4 pins which are dedicated for analog input and output functionality. The ADC and the DAC use the same reference voltage which is supplied by the PMIC LDO1 output to the VREF+ pin of the CPU. The LDO1 output is configured by default to 2.9 V output voltage.
The STM32MP1 provides two independent analog to digital converter with up to 16 bit resolution. ADC2 can also be used to monitor $V_{BAT}$, internal DAC1, internal DAC2 and the internal temperature sensor.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Range | Not used |
|---|---|---|---|---|---|---|
| AD0_IN | Analog input channel 0 | 8 | AIN | ANA0 | 0-2.9 V | - |
| AD1_IN | Analog input channel 1 | 6 | AIN | ANA1 | 0-2.9 V | - |
| AD2_IN | Analog input channel 2 / DAC_OUT1 | 4 | AINOUT | PA4_DAC_OUT1 | 0-2.9 V | - |
| AD3_IN | Analog input channel 3 / DAC_OUT2 | 2 | AINOUT | PA5_DAC_OUT2 | 0-2.9 V | - |

*Table 12: Analog inputs/outputs*

## 7.4 Touch controller

The DHCOM STM32MP1 module is equipped with a 4-Wire 12-bit resistive Touch Controller (Texas Instruments TSC2014), which is connected via I2C™ with the STM32MP1 processor.
The I2C™ device address of the touch controller is 0x49 (see also 7.8.3 Onboard I2C).

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| TSPX | Resistive Touch: 4 wire (X +) | 12 | AINOUT | - | PD |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| TSMX | Resistive Touch: 4 wire (X -) | 14 | AINOUT | - | PD |
| TSMY | Resistive Touch: 4 wire (Y -) | 16 | AINOUT | - | PD |
| TSPY | Resistive Touch: 4 wire (Y +) | 18 | AINOUT | - | PD |

*Table 13: Touch controller connections*

## 7.5 Audio / I2S

On the DHCOM STM32MP1 module the SAI interface is connected to the I2S pins. Therefore, the module provides next to the DHCOM I2S standard functionality some other standard protocols like AC'97 or PCM/DSP. The additional standards could also be used, but in this case, the customer loses the compatibility with the DHCOM family. This means, that the additional protocols are only guaranteed with the STM32MP1 processor modules.

The standard I2S interface has the following characteristics:

- Support for I2S master and slave mode
- Maximum audio sampling rate of 196kHz
- Compliant to Inter-IC Sound (I2S) bus specification from Philips

**Note:** The DHCOM I2S interface is connected to the STM32MP1 SAI2 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| I2S_RXFS | Receive Frame sync signal | 1 | I | PC0_SAI2_FS_B | - |
| I2S_RXD | Data receive signal | 5 | I | PF11_SAI2_SD_B | - |
| I2S_RXC | Receive clock signal | 7 | I | PH2_SAI2_SCK_B | - |
| I2S_TXFS | Transmit Frame sync signal | 11 | O | PI7_SAI2_FS_A | - |
| I2S_TXD | Data transmit signal | 15 | O | PI6_SAI2_SD_A | - |
| I2S_TXC | Transmit clock signal | 13 | O | PD13_SAI2_SCK_A | - |

*Table 14: Audio interface*

## 7.6 UART

The DHCOM STM32MP1 module provides three UART interfaces on the SODIMM connector. The DHCOM UART ports UART1 and UART2 are both implemented with CTS/RTS flow control. The DHCOM UART3 is used as UART interface without flow control.

The maximum transfer rate is 10Mbit/s.

### 7.6.1 UART 1

**Notes:**

- The DHCOM UART 1 interface is connected to the STM32MP1 UART4 interface.
- UART CTS and RTS signals are only available if CAN port 2 is not available. This means a module variant without option [–CAN2] must be used to support hardware handshake with DHCOM UART 1.

- It is essential to always create a possible connection to DHCOM UART 1, since the DHCOM bootloader can be operated with the UART 1. A minimum connection possibility should be made available via solder pads.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| UART1_CTS | UART clear to send | 24 | I | PB0_UART4_CTS | - |
| UART1_RTS | UART request to send | 26 | O | PA15_UART4_RTS | - |
| UART1_RX | UART receive data line | 32 | I | PB2_UART4_RX | - |
| UART1_TX | UART transmit data line | 34 | O | PG11_UART4_TX | - |

*Table 15: UART 1*

### 7.6.2 UART 2

**Note:** The DHCOM UART 2 interface is connected to the STM32MP1 UART8 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| UART2_CTS | UART clear to send | 31 | I | PG10_UART8_CTS | - |
| UART2_RTS | UART request to send | 33 | O | PG7_UART8_RTS | - |
| UART2_RX | UART receive data line | 35 | I | PE0_UART8_RX | - |
| UART2_TX | UART transmit data line | 37 | O | PE1_UART8_TX | - |

*Table 16: UART 2*

### 7.6.3 UART 3

**Note:** The DHCOM UART 3 interface is connected to the STM32MP1 UART3 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| UART3_RX | UART receive data line | 23 | I | PB12_USART3_RX | - |
| UART3_TX | UART transmit data line | 25 | O | PB10_USART3_TX | - |

*Table 17: UART 3*

## 7.7 SPI

The DHCOM STM32MP1 module is equipped with one SPI interface. The interface has the following characteristics:

- Up to 50 Mbit/s
- Full-duplex synchronous transfers on three lines
- 4-bit to 32-bit data size selection
- Multi master or multi slave mode capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- SPI Motorola and TI formats support
- ...

**Note:** The DHCOM SPI 1 interface is connected to the STM32MP1 SPI1 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| SPI1_CS0 | Slave select signal | 177 | O | PZ3_SPI1_NSS | - |
| SPI1_CLK | SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation) | 179 | IO | PZ0_SPI1_SCK | - |
| SPI1_MISO | SPI receive data line | 181 | I | PZ1_SPI1_MISO | - |
| SPI1_MOSI | SPI transmit data line | 183 | O | PZ2_SPI1_MOSI | - |

*Table 18: SPI 1*

## 7.8 I2C™

The DHCOM STM32MP1 module provides two external I2C™ interfaces on the SODIMM connector.

The I2C interfaces support standard (up to 100 Kbit/s), fast mode (up to 400 Kbit/s) and fast mode-plus (up to 1Mbit/s). They also support SMBus rev. 3.0 and PMBus rev. 1.3.

**Note:** The pull-up resistors required according to the I2CTM specification are already fitted on the module. For detailed information about I2CTM, reference is made to the specification (Philips Semiconductor):

http://www.nxp.com

### 7.8.1 I2C 1

**Note:** The DHCOM I2C 1 interface is connected to the STM32MP1 I2C5 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| I2C1_CLK | I²C clock line | 182 | IO | PA11_I2C5_SCL | - |
| I2C1_DATA | I²C data line | 184 | IO | PA12_I2C5_SDA | - |

*Table 19: I2C 1*

### 7.8.2 I2C 2

**Note:** The DHCOM I2C 2 interface is connected to the STM32MP1 I2C2 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| I2C2_CLK | I²C clock line | 158 | IO | PH4_I2C2_SCL | - |
| I2C2_DATA | I²C data line | 160 | IO | PH5_I2C2_SDA | - |

*Table 20: I2C 2*

### 7.8.3 Onboard I2C™

The onboard I2C interface is used to connect the following I2C devices:

| Device | | Address (7bit) |
|---|---|---|
| Touch Controller | TI TSC2014 | 0x49 |
| RTC | Micro Crystal RV-8803-C7 | 0x32 |
| EEPROM | Microchip 24AA025E48T-I/OT | 0x50 |
| PMIC | ST STPMIC1A | 0x33 |

*Table 21: Onboard I2C devices*

**Notes:**

- The onboard I2C interface is connected to the STM32MP1 I2C4 interface.
- The following CPU pins are used: PZ5_I2C4_SDA and PZ4_I2C4_SCL

# 7.9 CAN

The DHCOM STM32MP1 module supports both CAN modules (FDCAN1 and FDCAN2) of the STM32MP157 or STM32MP153. The interface supports the following main features:

- Compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A and B)
- Compliant with CAN FD protocol specification version 1.0
- CAN FD with max. 64 data bytes supported
- TTCAN protocol level 1 and level 2 completely in hardware (FDCAN1 only)
- Event synchronized time-triggered communication supported (FDCAN1 only)
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- Two configurable receive FIFOs
- Separate signaling on reception of high priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO /queue
- Configurable transmit event FIFO
- Both FDCAN1 and FDCAN2 modules share the same message RAM
- Programmable loop-back test mode
- Maskable module interrupts

## 7.9.1 CAN 1

**Note:** The DHCOM CAN 1 interface is connected to the STM32MP1 FDCAN1 interface.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| CAN_TX | CAN transmit data line | 27 | O | PH13_FDCAN1_TX | - |
| CAN_RX | CAN receive data line | 29 | I | PI9_FDCAN1_RX | - |

*Table 22: CAN 1*

## 7.9.2 CAN 2

**Notes:**

- The DHCOM CAN 2 interface is connected to the STM32MP1 FDCAN2 interface.
- DHCOM CAN 2 is only available if option [–CAN2] is selected in the specific variant. Then DHCOM UART1 hardware handshake (RTS and CTS) is not available.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| CAN2_TX | CAN transmit data line | 24 | O | PB13_FDCAN2_TX | - |
| CAN2_RX | CAN receive data line | 26 | I | PB5_FDCAN2_RX | - |

*Table 23: CAN 2*

# 7.10 Address-/Databus (FMC)

The STM32MP1 FMC interface (used in multiplexed asynchronous mode to access NOR flash memory) is connected through an address-latch to the SODIMM-200 socket. Therefore, the bus interface is after the address-latch as non-multiplexed bus interface available on the SODIMM-200 socket.

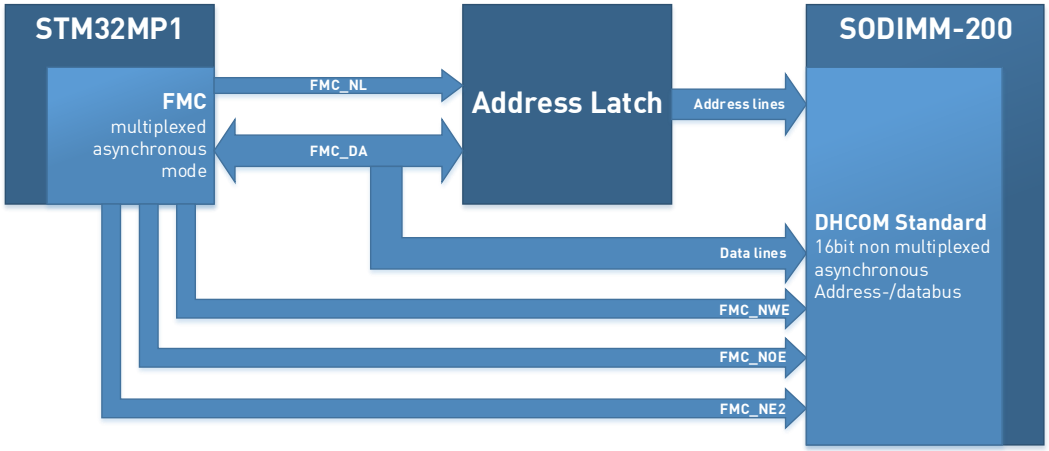


*Figure 7: Address-/Databus*

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| Vsysbus_OUT | System bus supply voltage output | 110 | PWR_O | - | - |
| A0 | Memory controller address line | 113 | O | Latch: PD14_FMC_DA0 | - |
| A1 | Memory controller address line | 115 | O | Latch: PD15_FMC_DA1 | - |
| A2 | Memory controller address line | 117 | O | Latch: PD0_FMC_DA2 | - |
| A3 | Memory controller address line | 119 | O | Latch: PD1_FMC_DA3 | - |
| A4 | Memory controller address line | 121 | O | Latch: PE7_FMC_DA4 | - |
| A5 | Memory controller address line | 123 | O | Latch: PE8_FMC_DA5 | - |
| A6 | Memory controller address line | 125 | O | Latch: PE9_FMC_DA6 | - |
| A7 | Memory controller address line | 127 | O | Latch: PE10_FMC_DA7 | - |
| A8 | Memory controller address line | 112 | O | Latch: PE11_FMC_DA8 | - |
| A9 | Memory controller address line | 114 | O | Latch: PE12_FMC_DA9 | - |
| A10 | Memory controller address line | 116 | O | Latch: PE13_FMC_DA10 | - |
| A11 | Memory controller address line | 118 | O | Latch: PE14_FMC_DA11 | - |
| A12 | Memory controller address line | 120 | O | Latch: PE15_FMC_DA12 | - |
| A13 | Memory controller address line | 122 | O | Latch: PD8_FMC_DA13 | - |
| A14 | Memory controller address line | 124 | O | Latch: PD9_FMC_DA14 | - |
| A15 | Memory controller address line | 126 | O | Latch: PD10_FMC_DA15 | - |
| D0 | Memory controller data line | 135 | IO | PD14_FMC_DA0 | - |
| D1 | Memory controller data line | 137 | IO | PD15_FMC_DA1 | - |
| D2 | Memory controller data line | 139 | IO | PD0_FMC_DA2 | - |
| D3 | Memory controller data line | 141 | IO | PD1_FMC_DA3 | - |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| D4 | Memory controller data line | 143 | IO | PE7_FMC_DA4 | - |
| D5 | Memory controller data line | 145 | IO | PE8_FMC_DA5 | - |
| D6 | Memory controller data line | 147 | IO | PE9_FMC_DA6 | - |
| D7 | Memory controller data line | 149 | IO | PE10_FMC_DA7 | - |
| D8 | Memory controller data line | 136 | IO | PE11_FMC_DA8 | - |
| D9 | Memory controller data line | 138 | IO | PE12_FMC_DA9 | - |
| D10 | Memory controller data line | 140 | IO | PE13_FMC_DA10 | - |
| D11 | Memory controller data line | 142 | IO | PE14_FMC_DA11 | - |
| D12 | Memory controller data line | 144 | IO | PE15_FMC_DA12 | - |
| D13 | Memory controller data line | 146 | IO | PD8_FMC_DA13 | - |
| D14 | Memory controller data line | 148 | IO | PD9_FMC_DA14 | - |
| D15 | Memory controller data line | 150 | IO | PD10_FMC_DA15 | - |
| CS_A | Static memory chip select 0 | 128 | O | PG12_FMC_NE4 | - |
| WE | Memory controller write enable | 133 | O | PD5_FMC_NWE | - |
| OE | Memory controller output enable | 134 | O | PD4_FMC_NOE | - |

*Table 24: Address-/Databus*

# 7.11 Display

## 7.11.1 RGB

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to WXGA (1366×768) @60 fps resolution with the following features:

- 2 display layers with dedicated FIFO
- Color look-up table (CLUT) up to 256 colors (256×24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| Vdisp_OUT | LCD controller supply voltage output | 46 | PWR_O | - | - |
| LC_R0 | LCD display data red 0 | 76 | O | PI15_LTDC_R0 | - |
| LC_R1 | LCD display data red 1 | 78 | O | PJ0_LTDC_R1 | - |
| LC_R2 | LCD display data red 2 | 49 | O | PJ1_LTDC_R2 | - |
| LC_R3 | LCD display data red 3 | 51 | O | PJ2_LTDC_R3 | - |
| LC_R4 | LCD display data red 4 | 53 | O | PJ3_LTDC_R4 | - |
| LC_R5 | LCD display data red 5 | 55 | O | PJ4_LTDC_R5 | - |
| LC_R6 | LCD display data red 6 | 57 | O | PJ5_LTDC_R6 | - |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| LC_R7 | LCD display data red 7 | 59 | O | PJ6_LTDC_R7 | - |
| LC_G0 | LCD display data green 0 | 80 | O | PJ7_LTDC_G0 | - |
| LC_G1 | LCD display data green 1 | 82 | O | PJ8_LTDC_G1 | - |
| LC_G2 | LCD display data green 2 | 61 | O | PJ9_LTDC_G2 | - |
| LC_G3 | LCD display data green 3 | 63 | O | PJ10_LTDC_G3 | - |
| LC_G4 | LCD display data green 4 | 65 | O | PJ11_LTDC_G4 | - |
| LC_G5 | LCD display data green 5 | 67 | O | PK0_LTDC_G5 | - |
| LC_G6 | LCD display data green 6 | 69 | O | PK1_LTDC_G6 | - |
| LC_G7 | LCD display data green 7 | 71 | O | PK2_LTDC_G7 | - |
| LC_B0 | LCD display data blue 0 | 84 | O | PJ12_LTDC_B0 | - |
| LC_B1 | LCD display data blue 1 | 86 | O | PJ13_LTDC_B1 | - |
| LC_B2 | LCD display data blue 2 | 73 | O | PJ14_LTDC_B2 | - |
| LC_B3 | LCD display data blue 3 | 75 | O | PJ15_LTDC_B3 | - |
| LC_B4 | LCD display data blue 4 | 77 | O | PK3_LTDC_B4 | - |
| LC_B5 | LCD display data blue 5 | 79 | O | PK4_LTDC_B5 | - |
| LC_B6 | LCD display data blue 6 | 81 | O | PK5_LTDC_B6 | - |
| LC_B7 | LCD display data blue 7 | 83 | O | PK6_LTDC_B7 | - |
| LC_EN | LCD display data enable | 85 | O | PK7_LTDC_DE | - |
| LC_VSYNC | LCD frame or vertical sync. pulse | 87 | O | PI13_LTDC_VSYNC | - |
| LC_HSYNC | LCD line or horizontal sync. pulse | 89 | O | PI12_LTDC_HSYNC | - |
| LC_PCLK | LCD pixel clock | 91 | O | PI14_LTDC_PCLK_F | - |
| GPIO_PWM | LCD contrast (only if PWM is not used) | 100 | O | PA3_TIM2_CH4_PWM_OUT | - |

*Table 25: RGB*

## 7.11.2 MIPI-DSI

The display serial interface (DSI) is part of a group of communication protocols defined by the MIPI® Alliance. The MIPI® DSI host controller is a digital core that implements all protocol functions defined in the MIPI® DSI specification. It provides an interface between the system and the MIPI® D-PHY, allowing the communication with a DSI-compliant display.

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS
- Supports up to two D-PHY data lanes at 1 Gbps
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports ultra-low-power mode with PLL disabled
- ECC and checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:

  - AMBA APB for control and optional support for generic and DCS commands
  - Video mode interface through LTDC
  - Adapted command mode interface through LTDC
  - Independently programmable virtual channel ID in video mode, adapted command mode and APB slave
- Video mode interfaces features:
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
  - Programmable polarity of all LTDC interface signals
  - Maximum resolution is limited by available DSI physical link bandwidth
- Adapted interface features:
  - Support for sending large amounts of data through the memory_write_start (WMS) and memory_write_continue (WMC) DCS commands
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
- Video mode pattern generator

**Note:** DHCOM DSI is only available if option [–DSI] is selected in the specific variant. Then DHCOM DSI interface is connected to the original DHCOM LVDS 1 connections.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| DSI_D0_P | DSI data0 differential signal positive line | 88 | IO | DSI_D0_P | - |
| DSI_D0_N | DSI data0 differential signal negative line | 90 | IO | DSI_D0_N | - |
| DSI_D1_P | DSI data1 differential signal positive line | 92 | O | DSI_D1_P | - |
| DSI_D1_N | DSI data1 differential signal negative line | 94 | O | DSI_D1_N | - |
| DSI_CK_P | DSI clock differential signal positive line | 97 | O | DSI_CK_P | - |
| DSI_CK_N | DSI clock differential signal negative line | 99 | O | DSI_CK_N | - |
| DSI_TE | ***Only available on request*** | 93 | I | PC6_DSI_TE | - |

*Table 26: MIPI DSI*

# 7.12 Camera

The digital camera is a synchronous parallel interface able to receive a high-speed data flow from an external 8-, 10-bit CMOS camera module. It supports the following main features:

- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Supports the following data formats:
  - 8/10-bit progressive video: either monochrome or raw bayer
  - YCbCr 4:2:2 progressive video
  - RGB 565 progressive video
  - Compressed data: JPEG

**Note:** If a MIPI® CSI-2 camera interface is needed, please have a look at the Avenger96 board as reference design (https://wiki.dh-electronics.com/index.php/Avenger96) with our DHCOR STM32MP1 module. On this design the camera interface is bridged using the STMIPID02 Chip from ST.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| $V_{CAM}$_OUT | Camera supply voltage output | 102 | PWR_O | - | - |
| CIF_D0 | Camera interface data line 0 | 48 | I | PH9_DCMI_D0 | - |
| CIF_D1 | Camera interface data line 1 | 50 | I | PH10_DCMI_D1 | - |
| CIF_D2 | Camera interface data line 2 | 52 | I | PH11_DCMI_D2 | - |
| CIF_D3 | Camera interface data line 3 | 54 | I | PH12_DCMI_D3 | - |
| CIF_D4 | Camera interface data line 4 | 56 | I | PH14_DCMI_D4 | - |
| CIF_D5 | Camera interface data line 5 | 58 | I | PI4_DCMI_D5 | - |
| CIF_D6 | Camera interface data line 6 | 60 | I | PB8_DCMI_D6 | - |
| CIF_D7 | Camera interface data line 7 | 62 | I | PE6_DCMI_D7 | - |
| CIF_D8 | Camera interface data line 8 | 64 | I | PI1_DCMI_D8 | - |
| CIF_D9 | Camera interface data line 9 | 66 | I | PH7_DCMI_D9 | - |
| CIF_VSYNC | Camera interface vertical synchronization | 68 | I | PI5_DCMI_VSYNC | - |
| CIF_MCLK | Camera interface reference clock **NOT AVAILABLE** with PG8. An external oscillator is needed. | 70 | O | PG8_GPIO_L | - |
| CIF_PCLK | Camera interface pixel clock | 72 | I | PA6_DCMI_PCLK | - |
| CIF_HSYNC | Camera interface horizontal synchronization | 74 | I | PH8_DCMI_HSYNC | - |

*Table 27: Camera*

# 7.13 PWM

The DHCOM STM32MP1 module enables the connection to Pulse Width Modulation output.

**Note:** The PWM output SODIMM pin 100 is typically used to control the Display backlight contrast.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| GPIO_PWM | PWM channel (only if LCD contrast is not used) | 100 | O | PA3_TIM2_CH4 | - |

*Table 28: PWM*

# 7.14 GPIOs

The DHCOM STM32MP1 module provides several GPIO pins on the SODIMM-200 socket.

**Notes:**

- Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHCOM standard.
- The DHCOM camera interface can also be used as alternative GPIO bank.
- After reset the multiplexer selection is alternate function 0 (AF0). The I/Os are configured in alternate function mode through GPIOx_MODER register. There the default value is "GPIO analog mode". After

reset, all GPIOs are in analog mode to reduce power consumption. Then also no pull-up or pull-down resistors are active.

- GPIO_A to GPIO_I and INT_HIGHEST_PRIORITY belongs to VIO_OUT. GPIO_J to GPIO_W belongs to VCAM_OUT. But in case of the DHCOM STM32MP1 module both voltage levels are 3V3.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| INT_HIGHEST_PRIORITY | Highest priority interrupt pin (active low) | 151 | IO | PI8_WKUP4 | PU |
| GPIO _A | General Purpose I/O | 154 | IO | PF3 | - |
| GPIO _B | General Purpose I/O | 156 | IO | PD6 | - |
| GPIO _C | General Purpose I/O | 162 | IO | PG0 | - |
| GPIO _D | General Purpose I/O | 163 | IO | PD12 | - |
| GPIO _E | General Purpose I/O | 164 | IO | PC6 | - |
| GPIO _F | General Purpose I/O | 165 | IO | PD11 | - |
| GPIO _G | General Purpose I/O | 167 | IO | PI0 | - |
| GPIO _H | General Purpose I/O | 173 | IO | PI2 | - |
| GPIO _I | General Purpose I/O | 175 | IO | PI3 | - |
| VIO_OUT | Voltage for external Level-Shifter | 152 | PWR_O | - | - |
| GPIO_J (or CIF_HSYNC) | General Purpose I/O | 74 | IO | PH8 | - |
| GPIO_K (or CIF_PCLK) | General Purpose I/O | 72 | IO | PA6 | - |
| GPIO_L (or CIF_MCLK) | General Purpose I/O | 70 | IO | PG8 | - |
| GPIO_M (or CIF_VSYNC) | General Purpose I/O | 68 | IO | PI5 | - |
| GPIO_N (or CIF_D9) | General Purpose I/O | 66 | IO | PH7 | - |
| GPIO_O (or CIF_D8) | General Purpose I/O | 64 | IO | PI1 | - |
| GPIO_P (or CIF_D7) | General Purpose I/O | 62 | IO | PE6 | - |
| GPIO_Q (or CIF_D6) | General Purpose I/O | 60 | IO | PB8 | - |
| GPIO_R (or CIF_D5) | General Purpose I/O | 58 | IO | PI4 | - |
| GPIO_S (or CIF_D4) | General Purpose I/O | 56 | IO | PH14 | - |
| GPIO_T (or CIF_D3) | General Purpose I/O | 54 | IO | PH12 | - |
| GPIO_U (or CIF_D2) | General Purpose I/O | 52 | IO | PH11 | - |
| GPIO_V (or CIF_D1) | General Purpose I/O | 50 | IO | PH10 | - |
| GPIO_W (or CIF_D0) | General Purpose I/O | 48 | IO | PH9 | - |
| Vcam_OUT | Voltage for external Level-Shifter | 102 | PWR_O | - | - |

*Table 29: GPIO's*

# 7.15 SD/MMC

For the SD card interface the SDIO port (SDMMC3) of the STM32MP157 is used. The interface is 4-bit wide and supports High Speed mode as maximum bus speed, due to 3V3 IO voltage level.

**Note:** The DHCOM SD interface is only available if the WiFi / Bluetooth module is not mounted.

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| SD_CLK | SD/SDIO/MMC bus clock | 103 | O | PG15_SDMMC3_CK | - |
| SD_CMD | SD/SDIO/MMC command line | 104 | IO | PF1_SDMMC3_CMD | - |

| SODIMM pin name | Description | SODIMM pin number | IO Type | CPU ball name | Not used |
|---|---|---|---|---|---|
| SD_DETECT | SD/SDIO/MMC card detection (active high) | 105 | I | PI10 | PU |
| SD_D0 | SD/SDIO/MMC data line | 106 | IO | PF0_SDMMC3_D0 | - |
| SD_D1 | SD/SDIO/MMC data line | 107 | IO | PF4_SDMMC3_D1 | - |
| SD_D2 | SD/SDIO/MMC data line | 108 | IO | PF5_SDMMC3_D2 | - |
| SD_D3 | SD/SDIO/MMC data line | 109 | IO | PD7_SDMMC3_D3 | - |

*Table 30: SD/MMC*

# 8 Onboard components

This chapter describes the onboard components. The used CPU connections are typically not available outside of the DHCOM module.

## 8.1 eMMC

As non-volatile data storage, the DHCOM STM32MP1 module provides an eMMC flash memory to store the operating system and application data on it. It is connected to the 8-bit SDMMC2 interface of the STM32MP1. The size of the eMMC can be between 4 GByte and 32 GByte and depends on the ordering configuration.

**Note:** eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly.

Please have a look at: https://en.wikipedia.org/wiki/Flash_memory#Write_endurance

| Description | IO Type | CPU ball name |
|---|---|---|
| SDMMC bus clock | O | PE3_SDMMC2_CK |
| SDMMC command line | O | PG6_SDMMC2_CMD |
| SDMMC data line 0 | IO | PB14_SDMMC2_D0 |
| SDMMC data line 1 | IO | PB15_SDMMC2_D1 |
| SDMMC data line 2 | IO | PB3_SDMMC2_D2 |
| SDMMC data line 3 | IO | PB4_SDMMC2_D3 |
| SDMMC data line 4 | IO | PA8_SDMMC2_D4 |
| SDMMC data line 5 | IO | PA9_SDMMC2_D5 |
| SDMMC data line 6 | IO | PE5_SDMMC2_D6 |
| SDMMC data line 7 | IO | PD3_SDMMC2_D7 |

*Table 31: eMMC*

## 8.2 DDR3

The DHCOM STM32MP1 module provides up to 1 GByte DDR3L SDRAM. The memory is connected via a 32 bit wide data bus und may be clocked up to 533 MHz. The DDR3L memory size can be between 256 Mbyte and 1 GByte and depends on the ordering configuration.

## 8.3 SPI boot flash

The DHCOM STM32MP1 module provides a 2 Mbyte Quad SPI NOR boot flash. By default, the boot mode is set to serial NOR boot and the 2 Mbyte flash memory contains a preprogrammed standard bootloader.

After power on the STM32MP1 ROM code starts up and loads the bootloader from the Quad SPI NOR flash. The bootloader can afterwards start the operating system from other flash devices like eMMC or SD card.

| Description | IO Type | CPU ball name |
|---|---|---|
| Slave select signal | O | PB6_QSPI_BK1_NCS |
| SPI clock line | O | PF10_QSPI_CLK |
| Quad SPI IO0 | IO | PF8_QSPI_BK1_IO0 |
| Quad SPI IO1 | IO | PF9_QSPI_BK1_IO1 |
| Quad SPI IO2 | IO | PF7_QSPI_BK1_IO2 |
| Quad SPI IO3 | IO | PF6_QSPI_BK1_IO3 |

*Table 32: Quad SPI NOR flash*

## 8.4 WiFi / Bluetooth

The DHCOM STM32MP1 module is available with the optional onboard WiFi and Bluetooth module RS9116N-DB00-CC1 from Redpine Signals.

Redpine Signals RS9116 dual band CC1 module provide a comprehensive multi-protocol wireless connectivity solution including IEEE 802.11 a/b/g/n (2.4GHz and 5GHz), 802.11j, dual-mode Bluetooth 5. The module offers high throughput, extended range with power-optimized performance. The modules are FCC, IC, and ETSI/CE certified. Redpine offers drivers for high-level operating systems such as Linux.

### 8.4.1 Features

**Wi-Fi:**

- Compliant to single-spatial stream IEEE 802.11 a/b/g/n, 802.11j (hosted mode) with dual band (2.4 and 5 GHz in CC1 module) support
- Support for 20 MHz and 40 MHz channel bandwidths
- Transmit power up to +18dBm in 2 GHz and +13.5 dBm in 5 GHz
- Receive sensitivity as low as -96 dBm in 2 GHz and - 89 dBm in 5 GHz
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g/a: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz - 2484 MHz, 4.9 GHz - 5.975 GHz

**Bluetooth:**

- Compliant to dual-mode Bluetooth 5
- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity: -92 dBm, LR 125 Kbps: -102 dBm
- < 8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2Mbps, 3 Mbps
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- EDR+2.1, 4.0, 4.1, 4.2 and 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long-Range modes
- Bluetooth Low Energy Secure connections.
- Bluetooth auto rate and auto TX power adaptation

- Piconet with Seven active logical links. Scatternet with two slave roles while still being visible.
- Bluetooth inbuilt stack support for L2CAP, AVDTP, AVCTP, RFCOMM, SDP, ATT, SMP
- Bluetooth profile support for SPP, A2DP, AVRCP, HFP, PBAP, IAP, GAP, GATT, IAP1, IAP2, HID

**RF Features:**

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch
- Integrated Antenna and u.FL connector
- Diversity is supported

**Power Consumption:**

- Wi-Fi Standby Associated mode current: 40uA @ 1 second beacon listen interval
- Wi-Fi 1 Mbps Listen current: 14 mA
- Wi-Fi LP chain Rx current: 19 mA
- Deep sleep current <1 uA, Standby current (RAM retention) < 10 uA

**Security:**

- Hardware device identity and key storage with PUF based secure Roots-of-trust (RoT)
- Accelerators: AES128/256, SHA256/384/512, HMAC, RSA, ECC, ECDH, RNG, CRC
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client, EAP-TLS, EAP-FAST, EAP-TTLS, EAP-LEAP, PEAP-MSCHAP-v2
- True Random Number Generator
- Secure Boot
- Secure Firmware upgrade with backup
- FIPS140-2 compliant

### 8.4.2 Used STM32MP1 CPU signals

**Notes:**

- If WiFi / Bluetooth module is mounted, the DHCOM SD interface is not available.
- The WiFi / Bluetooth module is connected to the STM32MP1 via the SDIO interface only. This includes both, WiFi and Bluetooth.

| Description | IO Type | CPU ball name |
|---|---|---|
| SDIO bus clock | O | PG15_SDMMC3_CK |
| SDIO command line | O | PF1_SDMMC3_CMD |
| SDIO data line 0 | IO | PF0_SDMMC3_D0 |
| SDIO data line 1 | IO | PF4_SDMMC3_D1 |
| SDIO data line 2 | IO | PF5_SDMMC3_D2 |
| SDIO data line 3 | IO | PD7_SDMMC3_D3 |

*Table 33: SDIO for WiFi / Bluetooth*

## 8.5 RTC

The DHCOM STM32MP1 module is available with the optional onboard temperature compensated RTC RV-8803-C7 from Micro Crystal. The RTC is connected to the STM32MP1 I2C4 port. Please also have a look at chapter 7.8.3 “Onboard I2C™”.

The RTC can be supplied during time keeping mode via a Goldcap or a button cell battery. Therefore, the supply voltage can be applied through the VCC_BAT SODIMM-200 connection. Please have also a look at chapter 4 “Power supply and reset”.

**Features:**

- Factory calibrated temperature compensation
- Very high Time Accuracy (best in class).
  - ±1.5 ppm 0 to +50°C
  - ±3.0 ppm -40 to +85°C
  - ±7.0 ppm +85 to +105°C
- Low power consumption: 240 nA @ 3 V. (best in class)
- Wide operating voltage range: 1.5 V to 5.5 V.
- Aging compensation with OFFSET value
- Counters for hundredths of seconds, seconds, minutes, hours, date, month, year and weekday
- Operating temperature range: -40 to +105°C

## 8.6 EEPROM

### 8.6.1 EEPROM for ETH 1

The MAC address of the Ethernet 1 controller is stored in the 2 Kbit sized EEPROM (24AA025E48T-I/OT) from Microchip. It is connected to the onboard I2C-Interface (see 7.8.3 Onboard I2CTM) and is reachable at the 7 bit address 0x50. It can also be used to store additional data on it. However, only the addresses from 0x00 to 0x80 are user accessible.

The MAC-address itself is stored inside the permanently write protected area of the EEPROM on the addresses 0xFA to 0xFF.

### 8.6.2 EEPROM for ETH 2

The second EEPROM is connected via a SPI interface directly to the KSZ8851 ethernet controller (see 7.1.2 ETH2) and therefore it is only accessible by the KSZ8851. Since it cannot be accessed without the ethernet controller, it is only available when choosing the DHCOM STM32MP1 with the option [-E2] for the second ethernet port.

Also, this EEPROM is used to store the MAC address inside of it, but take note, that it has no permanent write protection which means, that the end-application must ensure, that the MAC address is not changed by accident. The MAC address is located at the addresses 0x01 to 0x03 (16-bit mode).

## 8.7 microSD socket

The onboard microSD socket is connected to SDIO port (SDMMC1) of the STM32MP1 which can be used as a boot source (see 6 Boot Mode). This socket is only populated when ordering the DHCOM STM32MP1 with the option [-SD] or [-SDR104].
With the option [-SD] the microSD socket supports microSD cards compliant to the "high speed" classification. For applications which require a faster access to the microSD card, the DHCOM STM32MP1 can be ordered with the option [-SDR104], in which an additional microSD level translator is added in order to support SDR104 bus speed grade.

| Description | IO Type | CPU ball name |
|---|---|---|
| SDIO bus clock | O | PC12_SDMMC1_CK |
| SDIO bus clock feedback | I | PE4_SDMMC1_CKIN |
| SDIO command line | IO | PD2_SDMMC1_CMD |
| SDIO direction control for command | O | PB9_SDMMC1_CDIR |
| SDIO data line 0 | IO | PC8_SDMMC1_D0 |
| SDIO data line 1 | IO | PC9_SDMMC1_D1 |
| SDIO data line 2 | IO | PC10_SDMMC1_D2 |
| SDIO data line 3 | IO | PC11_SDMMC1_D3 |
| SDIO direction control for data line 0 | O | PF2_SDMMC1_D0DIR |
| SDIO direction control for data lines 1 to 3 | O | PC7_SDMMC1_D123DIR |
| SDIO card side IO selection | O | PF14_uSD_SEL_LDO |

*Table 34:SDIO for the microSD socket*

# 9 Plugs and connections

## 9.1 SODIMM-200

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 1 | I2S_RXFS | PC0 | VIO |
| 3 | Microphone GND | - | VDDA |
| 5 | I2S_RXD | PF11 | VIO |
| 7 | I2S_RXC | PH2 | VIO |
| 9 | Audio GND | - | VDDA |
| 11 | I2S_TXFS | PI7 | VIO |
| 13 | I2S_TXC | PD13 | VIO |
| 15 | I2S_TXD | PI6 | VIO |
| 17 | GND1 | - | Vin |
| 19 | GND2 | - | Vin |
| 21 | RESET_IN | - | VIO |
| 23 | UART3_RX | PB12 | VIO |
| 25 | UART3_TX | PB10 | VIO |
| 27 | CAN_TX | PH13 | VIO |
| 29 | CAN_RX | PI9 | VIO |
| 31 | UART2_CTS | PG10 | VIO |
| 33 | UART2_RTS | PG7 | VIO |
| 35 | UART2_RX | PE0 | VIO |
| 37 | UART2_TX | PE1 | VIO |
| 39 | VCC_IN2 | - | Vin |
| 41 | VCC_IN4 | - | Vin |
| 43 | GND3 | - | Vin |
| 45 | GND4 | - | Vin |
| 47 | GND5 | - | Vin |
| 49 | LC_R2 | PJ1 | Vdisp |
| 51 | LC_R3 | PJ2 | Vdisp |
| 53 | LC_R4 | PJ3 | Vdisp |
| 55 | LC_R5 | PJ4 | Vdisp |
| 57 | LC_R6 | PJ5 | Vdisp |
| 59 | LC_R7 | PJ6 | Vdisp |
| 61 | LC_G2 | PJ9 | Vdisp |
| 63 | LC_G3 | PJ10 | Vdisp |
| 65 | LC_G4 | PJ11 | Vdisp |
| 67 | LC_G5 | PK0 | Vdisp |
| 69 | LC_G6 | PK1 | Vdisp |
| 71 | LC_G7 | PK2 | Vdisp |
| 73 | LC_B2 | PJ14 | Vdisp |

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 2 | Analog Input 3 | PA5 | PMIC_VDDA[1] |
| 4 | Analog Input 2 | PA4 | PMIC_VDDA[1] |
| 6 | Analog Input 1 | ANA1 | PMIC_VDDA[1] |
| 8 | Analog Input 0 | ANA0 | PMIC_VDDA[1] |
| 10 | VDDA[2] | - | VDDA |
| 12 | TSPX | - | VIO |
| 14 | TSMX | - | VIO |
| 16 | TSMY | - | VIO |
| 18 | TSPY | - | VIO |
| 20 | RESET_OUT | - | VIO |
| 22 | *Reserved* | - | VIO |
| 24 | UART1_CTS or CAN2_TX[3] | PB0/PB13 | VIO |
| 26 | UART1_RTS or CAN2_RX[3] | PA15/PB5 | VIO |
| 28 | *Reserved* | - | VIO |
| 30 | *Reserved* | - | VIO |
| 32 | UART1_RX | PB2 | VIO |
| 34 | UART1_TX | PG11 | VIO |
| 36 | *Reserved* | - | VIO |
| 38 | VCC_IN1 | - | Vin |
| 40 | VCC_IN3 | - | Vin |
| 42 | VCC_IN5 | - | Vin |
| 44 | VCC_IN6 | - | Vin |
| 46 | Vdisp_OUT | - | Vdisp |
| 48 | GPIO_W alt. CIF_D0[4] | PH9 | Vcam |
| 50 | GPIO_V alt. CIF_D1[4] | PH10 | Vcam |
| 52 | GPIO_U alt. CIF_D2[4] | PH11 | Vcam |
| 54 | GPIO_T alt. CIF_D3[4] | PH12 | Vcam |
| 56 | GPIO_S alt. CIF_D4[4] | PH14 | Vcam |
| 58 | GPIO_R alt. CIF_D5[4] | PI4 | Vcam |
| 60 | GPIO_Q alt. CIF_D6[4] | PB8 | Vcam |
| 62 | GPIO_P alt. CIF_D7[4] | PE6 | Vcam |
| 64 | GPIO_O alt. CIF_D8[4] | PI1 | Vcam |
| 66 | GPIO_N alt. CIF_D9[4] | PH7 | Vcam |
| 68 | GPIO_M alt. CIF_VSYNC[4] | PI5 | Vcam |
| 70 | GPIO_L alt. CIF_MCLK[4] | PG8 | Vcam |
| 72 | GPIO_K alt. CIF_PCLK[4] | PA6 | Vcam |
| 74 | GPIO_J alt. CIF_HSYNC[4] | PH8 | Vcam |

[1] PMIC_VDDA is connected to the LDO1 of the PMIC (STPMIC1A). As a standard, this reference voltage is set to 2.9 V. (See 7.3 ADC / DAC)
[2] On the DHCOM STM32MP1 VDDA is not used, because the module is not available with onboard Audio Codec. (See 4.1.4 Signal Overview)
[3] CTS and RTS is only available if option [-CAN2] is not selected. (See 7.6.1 UART 1 and 7.9.2 CAN 2)
[4] When the camera interface is not needed, these pins can be used as GPIOs. (See 7.12 Camera and 7.14 GPIOs)

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 75 | LC_B3 | PJ15 | Vdisp |
| 77 | LC_B4 | PK3 | Vdisp |
| 79 | LC_B5 | PK4 | Vdisp |
| 81 | LC_B6 | PK5 | Vdisp |
| 83 | LC_B7 | PK6 | Vdisp |
| 85 | LC_EN | PK7 | Vdisp |
| 87 | LC_VSYNC | PI13 | Vdisp |
| 89 | LC_HSYNC | PI12 | Vdisp |
| 91 | LC_PCLK | PI14 | Vdisp |
| 93 | *DSI_TE (Only on request)* | *PC6* | DSI |
| 95 | *Reserved* | - | DSI |
| 97 | DSI_CK_P[5] | DSI_CK_P | DSI |
| 99 | DSI_CK_N[5] | DSI_CK_N | DSI |
| 101 | GND6 | - | Vin |
| 103 | SD_CLK[6] | PG15 | VIO |
| 105 | SD_DETECT[6] | PI10 | VIO |
| 107 | SD_D1[6] | PF4 | VIO |
| 109 | SD_D3[6] | PD7 | VIO |
| 111 | GND7 | - | Vin |
| 113 | A0[7] | PD14 | Vsysbus |
| 115 | A1[7] | PD15 | Vsysbus |
| 117 | A2[7] | PD0 | Vsysbus |
| 119 | A3[7] | PD1 | Vsysbus |
| 121 | A4[7] | PE7 | Vsysbus |
| 123 | A5[7] | PE8 | Vsysbus |
| 125 | A6[7] | PE9 | Vsysbus |
| 127 | A7[7] | PE10 | Vsysbus |
| 129 | *Reserved* | - | Vsysbus |
| 131 | *Reserved* | - | Vsysbus |
| 133 | WE | PD5 | Vsysbus |
| 135 | D0 | PD14 | Vsysbus |
| 137 | D1 | PD15 | Vsysbus |
| 139 | D2 | PD0 | Vsysbus |
| 141 | D3 | PD1 | Vsysbus |
| 143 | D4 | PE7 | Vsysbus |
| 145 | D5 | PE8 | Vsysbus |
| 147 | D6 | PE9 | Vsysbus |
| 149 | D7 | PE10 | Vsysbus |
| 151 | INT_HIGHEST_PRIORITY | PI8 | VIO |
| 153 | GND8 | - | Vin |
| 155 | *Reserved* | - | VIO |
| 157 | *Reserved* | - | VIO |
| 159 | *Reserved* | - | VIO |

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 76 | LC_R0 | PI15 | Vdisp |
| 78 | LC_R1 | PJ0 | Vdisp |
| 80 | LC_G0 | PJ7 | Vdisp |
| 82 | LC_G1 | PJ8 | Vdisp |
| 84 | LC_B0 | PJ12 | Vdisp |
| 86 | LC_B1 | PJ13 | Vdisp |
| 88 | DSI_D0_P[5] | DSI_D0_P | DSI |
| 90 | DSI_D0_N[5] | DSI_D0_N | DSI |
| 92 | DSI_D1_P[5] | DSI_D1_P | DSI |
| 94 | DSI_D1_N[5] | DSI_D1_N | DSI |
| 96 | *Reserved* | - | DSI |
| 98 | *Reserved* | - | DSI |
| 100 | GPIO_PWM | PA3 | VIO |
| 102 | Vcam_OUT | - | Vcam |
| 104 | SD_CMD[6] | PF1 | VIO |
| 106 | SD_D0[6] | PF0 | VIO |
| 108 | SD_D2[6] | PF5 | VIO |
| 110 | Vsysbus_OUT | - | Vsysbus |
| 112 | A8[7] | PE11 | Vsysbus |
| 114 | A9[7] | PE12 | Vsysbus |
| 116 | A10[7] | PE13 | Vsysbus |
| 118 | A11[7] | PE14 | Vsysbus |
| 120 | A12[7] | PE15 | Vsysbus |
| 122 | A13[7] | PD8 | Vsysbus |
| 124 | A14[7] | PD9 | Vsysbus |
| 126 | A15[7] | PD10 | Vsysbus |
| 128 | CS_A | PG12 | Vsysbus |
| 130 | *Reserved* | - | Vsysbus |
| 132 | *Reserved* | - | Vsysbus |
| 134 | OE | PD4 | Vsysbus |
| 136 | D8 | PE11 | Vsysbus |
| 138 | D9 | PE12 | Vsysbus |
| 140 | D10 | PE13 | Vsysbus |
| 142 | D11 | PE14 | Vsysbus |
| 144 | D12 | PE15 | Vsysbus |
| 146 | D13 | PD8 | Vsysbus |
| 148 | D14 | PD9 | Vsysbus |
| 150 | D15 | PD10 | Vsysbus |
| 152 | VIO_OUT | - | VIO |
| 154 | GPIO_A | PF3 | VIO |
| 156 | GPIO_B | PD6 | VIO |
| 158 | I2C2_CLK | PH4 | VIO |
| 160 | I2C2_DATA | PH5 | VIO |

[5] DSI is only available when ordering a DHCOM STM32MP1 with the option [-DSI]. (See 7.11.2 MIPI-DSI)
[6] The SD interface on the SODIMM-200 connector is only available when WiFi / Bluetooth module is not mounted. (See 7.15 SD/MMC)
[7] The Address lines (A0 to A15) are connected via an address latch to the SODIMM-200. (See 7.10 Address-/Databus (FMC))

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 161 | *Reserved* | - | VIO |
| 163 | GPIO_D | PD12 | VIO |
| 165 | GPIO_F | PD11 | VIO |
| 167 | GPIO_G | PI0 | VIO |
| 169 | *Reserved* | - | USB |
| 171 | *Reserved* | - | USB |
| 173 | GPIO_H | PI2 | VIO |
| 175 | GPIO_I | PI3 | VIO |
| 177 | SPI1_CS0 | PZ3 | VIO |
| 179 | SPI1_CLK | PZ0 | VIO |
| 181 | SPI1_MISO | PZ1 | VIO |
| 183 | SPI1_MOSI | PZ2 | VIO |
| 185 | GND9 | - | Vin |
| 187 | nETH2_LINK_LED | - | VIO |
| 189 | nETH2_SPEED_LED | - | VIO |
| 191 | ETH2_TXI- | - | Ethernet |
| 193 | ETH2_TXI+ | - | Ethernet |
| 195 | ETH2_RXI- | - | Ethernet |
| 197 | ETH2_RXI+ | - | Ethernet |
| 199 | GND10 | - | Vin |

| Pin number | Pin name | CPU Pin | Power domain |
|---|---|---|---|
| 162 | GPIO_C | PG0 | VIO |
| 164 | GPIO_E | PC6 | VIO |
| 166 | USB_OTG_VBUS | OTG_VBUS | USB |
| 168 | USB_OTG_ID | PA10 | VIO |
| 170 | USB_OTG_D+ | USB_DP2 | USB |
| 172 | USB_OTG_D- | USB_DM2 | USB |
| 174 | USB_PWR_STAT | PA14 | VIO |
| 176 | USB_PWR_EN | PA13 | VIO |
| 178 | USB_HOST_D1+ | USB_DP1 | USB |
| 180 | USB_HOST_D1- | USB_DM1 | USB |
| 182 | I2C1_CLK | PA11 | VIO |
| 184 | I2C1_DATA | PA12 | VIO |
| 186 | nETH1_LINK_LED[8] | - | VIO |
| 188 | nETH1_SPEED_LED[8] | - | VIO |
| 190 | ETH1_TXD-[8] | - | Ethernet |
| 192 | ETH1_TXD+[8] | - | Ethernet |
| 194 | ETH_VIO_SWITCHED[8] | - | VIO |
| 196 | ETH1_RXI-[8] | - | Ethernet |
| 198 | ETH1_RXI+[8] | - | Ethernet |
| 200 | VCC_BAT | - | Vbat |

*Table 35: SODIMM-200 pin assignment*

## 9.2 DHCOM-X

| Pin number | Pin name | CPU Pin | Voltage level |
|---|---|---|---|
| 1 | RGMII_RXCLK[8] | PA1 | Vrgmii |
| 3 | RGMII_RXD0[8] | PC4 | Vrgmii |
| 5 | RGMII_RXD1[8] | PC5 | Vrgmii |
| 7 | RGMII_RXD2[8] | PH6 | Vrgmii |
| 9 | RGMII_RXD3[8] | PB1 | Vrgmii |
| 11 | RGMII_RX_CTL[8] | PA7 | Vrgmii |
| 13 | RGMII_MDIO[8] | PA2 | Vrgmii |
| 15 | RGMII_RST[8] | PH3 | Vrgmii |
| 17 | *Reserved* | - | 3V3 |
| 19 | GND | - | Vin |
| 21 | *Reserved* | - | Sata |
| 23 | *Reserved* | - | Sata |
| 25 | GND | - | Vin |
| 27 | *Reserved* | - | PCIe |
| 29 | *Reserved* | - | PCIe |
| 31 | *Reserved* | - | PCIe |
| 33 | *Reserved* | - | PCIe |

| Pin number | Pin name | CPU Pin | Voltage level |
|---|---|---|---|
| 2 | RGMII_TXCLK[8] | PG4 | Vrgmii |
| 4 | RGMII_TXD0[8] | PG13 | Vrgmii |
| 6 | RGMII_TXD1[8] | PG14 | Vrgmii |
| 8 | RGMII_TXD2[8] | PC2 | Vrgmii |
| 10 | RGMII_TXD3[8] | PE2 | Vrgmii |
| 12 | RGMII_TX_CTL[8] | PB11 | Vrgmii |
| 14 | RGMII_MDC[8] | PC1 | Vrgmii |
| 16 | RGMII_REFCLK[8] | PG5 | Vrgmii |
| 18 | RGMII_INT[8] | PI11 | 3V3 |
| 20 | VCC_RGMII_OUT[8] | - | Vrgmii |
| 22 | GND | - | Vin |
| 24 | *Reserved* | - | Sata |
| 26 | *Reserved* | - | Sata |
| 28 | GND | - | Vin |
| 30 | *Reserved* | - | PCIe |
| 32 | *Reserved* | - | PCIe |
| 34 | *Reserved* | - | 3V3 |

[8] Ethernet 1 is only available when ordering a DHCOM STM32MP1 without the RGMII interface (option [-HS]) and vice versa. (See 7.1 Ethernet)

| Pin number | Pin name | CPU Pin | Voltage level | Pin number | Pin name | CPU Pin | Voltage level |
|---|---|---|---|---|---|---|---|
| 35 | GND | - | Vin | 36 | GND | - | Vin |
| 37 | *Reserved* | - | CSI | 38 | *Reserved* | - | CSI |
| 39 | *Reserved* | - | CSI | 40 | *Reserved* | - | CSI |
| 41 | GND | - | Vin | 42 | *Reserved* | - | CSI |
| 43 | *Reserved* | - | HDMI | 44 | *Reserved* | - | CSI |
| 45 | *Reserved* | - | HDMI | 46 | GND | - | Vin |
| 47 | *Reserved* | - | HDMI | 48 | *Reserved* | - | HDMI |
| 49 | *Reserved* | - | HDMI | 50 | *Reserved* | - | HDMI |
| 51 | *HDMI_CEC (Only on request)* | *PA15* | 2V5 | 52 | *Reserved* | - | HDMI |
| 53 | GND | | Vin | 54 | *Reserved* | - | HDMI |
| 55 | *DSI_CK_P (Only on request)* | *DSI_CK_P* | LVDS | 56 | *Reserved* | - | 2V5 |
| 57 | *DSI_CK_N (Only on request)* | *DSI_CK_N* | LVDS | 58 | GND | - | Vin |
| 59 | *DSI_TE (Only on request)* | *PC6* | LVDS | 60 | *DSI_D0_P (Only on request)* | *DSI_D0_P* | LVDS |
| 61 | *Reserved* | - | LVDS | 62 | *DSI_D0_N (Only on request)* | *DSI_D0_N* | LVDS |
| 63 | *Reserved* | - | LVDS | 64 | *DSI_D1_P (Only on request)* | *DSI_D1_P* | LVDS |
| 65 | *Reserved* | - | LVDS | 66 | *DSI_D1_N (Only on request)* | *DSI_D1_N* | LVDS |
| 67 | GND | - | Vin | 68 | GND | - | Vin |
| 69 | *Reserved* | - | - | 70 | *Reserved* | - | - |
| 71 | *Reserved* | - | - | 72 | *Reserved* | - | - |
| 73 | *Reserved* | - | - | 74 | *Reserved* | - | - |
| 75 | *Reserved* | - | - | 76 | *Reserved* | - | - |
| 77 | *Reserved* | - | - | 78 | *Reserved* | - | - |
| 79 | VCC_IN7 | - | Vin | 80 | VCC_IN8 | - | Vin |

*Table 36: DHCOM-X connector pin assignment*

## 9.3 JTAG and SWD

The STM32MP1 DHCOM Module supports JTAG and SWD. Both interfaces are accessible at the same connectors and therefore the function is depending on the current mode.

### 9.3.1 FFC connector

| Pin number | Pin name (JTAG-Mode) | Pin name (SWD-Mode) |
|---|---|---|
| 1 | +3V3 Output | +3V3 Output |
| 2 | GND | GND |
| 3 | JTAG_TMS | SWDIO |
| 4 | #JTAG_TRST | #TRST |
| 5 | JTAG_TCK | SWCLK |
| 6 | JTAG_TDO | SWO |
| 7 | JTAG_TDI | *Reserved* |
| 8 | #RESET_IN | #RESET_IN |
| 9 | *Reserved* | *Reserved* |
| 10 | *Reserved* | *Reserved* |

*Table 37: FFC JTAG interface pin assignment*

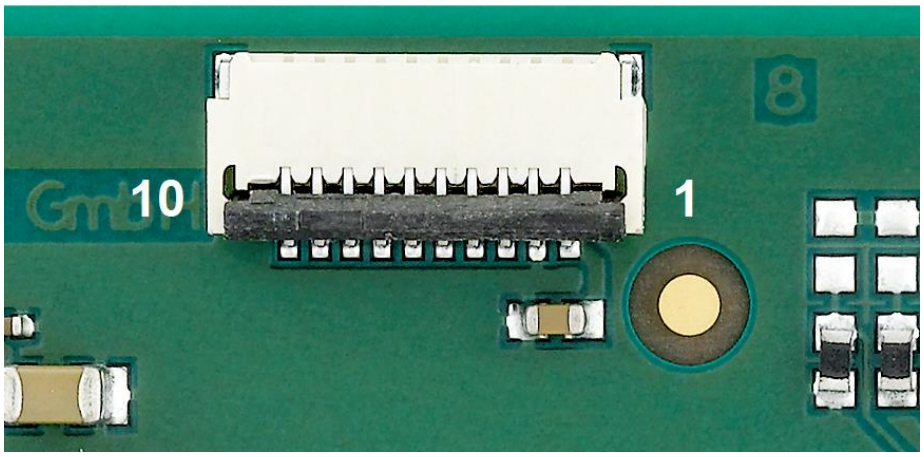


*Figure 8: Pin assignment of the FFC JTAG connector which has top and bottom contacts (Würth Elektronik: 687110182122)*

### 9.3.2 TAG-Connect

| Pin number | Pin name (JTAG-Mode) | Pin name (SWD-Mode) |
|---|---|---|
| 1 | +3V3 Output | +3V3 Output |
| 2 | JTAG_TMS | SWDIO |
| 3 | GND | GND |
| 4 | JTAG_TCK | SWCLK |
| 5 | GND | GND |
| 6 | JTAG_TDO | SWO |
| 7 | *Reserved* | *Reserved* |
| 8 | JTAG_TDI | *Reserved* |
| 9 | #JTAG_TRST | #TRST |
| 10 | #RESET_IN | #RESET_IN |

*Table 38: Tag-Connect JTAG interface pin assignment*

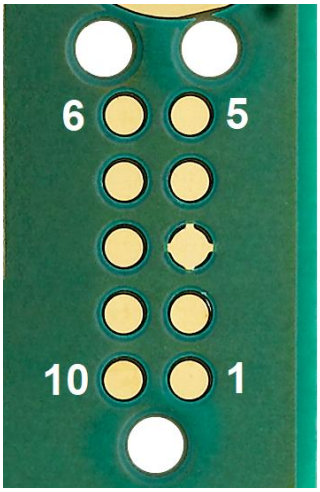


*Figure 9: TAG Connect pin assignment on the topside of the DHCOM STM32MP1 to use with a TC2050-IDC-NL cable*

# 10 Technical specifications

## 10.1 Operating conditions – Absolute maximum ratings

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCC (Vin) | Power supply voltage INPUT | 3.2 | | 5.5 | V |
| $VCC_{ripple}$ (Vin) | VCC ripple peak-to-peak | | 50 | 100 | mV |
| $V_{bat}$ | Internal RTC; Battery voltage INPUT | 1.4 | | 3.6 | V |
| $V_{bat}$ | External RTC; Battery voltage INPUT (option [-RTC]) | 1.3 | | 4.0 | V |
| $V_{sysbus}$ | System bus voltage OUTPUT | | 3.3 | | V |
| $I_{Vsysbus}$ | Vsysbus current | | | 20 | mA |
| $V_{disp}$ | Display voltage OUTPUT | | 3.3 | | V |
| $I_{Vdisp}$ | Vdisp current | | | 20 | mA |
| $V_{cam}$ | Camera voltage OUTPUT | | 3.3 | | V |
| $I_{Vcam}$ | Vcam current | | | 20 | mA |
| $V_{IO}$ | I/O voltage OUTPUT | | 3.3 | | V |
| $I_{VIO}$ | VIO current | | | 20 | mA |
| $V_{ETH\_VIO\_SWITCHED}$ | ETH_VIO_SWITCHED voltage OUTPUT | | 3.3 | | V |
| $I_{ETH\_VIO\_SWITCHED}$ | ETH_VIO_SWITCHED current | | | 60 | mA |
| IVbat | External RTC; Vbat input current (Vbat = 3.0 V) (option [-RTC]) | | 5 | 40 | µA |
| IVbat_Stby | External RTC; Vbat Standby input current (Vbat = 3.0 V) (option [-RTC]) | | 240 | 600 | nA |
| VIH_3V3 | Digital input high voltage | 2.0 | 3.3 | | V |
| VIL_3V3 | Digital input low voltage | | 0 | 0.8 | V |

*Table 39: DC operating conditions*

## 10.2 Operating conditions – Power examples

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $P_{STM32MP157\_IDLE}$ | Power consumption of dual core variant (650 MHz) in Idle mode; VCC (Vin) = 3.3 V[9] | | 1.4 | | W |
| $P_{STM32MP157\_STRESS\_TEST}$ | Power consumption of dual core variant (650 MHz) during stress test; VCC (Vin) = 3.3 V[10] | | 2.0 | 2.4 | W |
| $P_{STM32MP157\_IDLE}$ | Power consumption of dual core variant with GPU (650 MHz) in Idle mode with; VCC (Vin) = 5 V[9] | | 1.6 | | W |
| $P_{STM32MP157\_STRESS\_TEST}$ | Power consumption of dual core variant with GPU (650 MHz) during stress test; VCC (Vin) = 5 V[10] | | 2.1 | 2.6 | W |

*Table 40: Power examples*

[9] Test condition „idle": DHCOM STM32MP1 (587-100) variant HS00014 (with WiFi/Bluetooth module and two Ethernet Phys) inside PDK2 (516-400) with all jumpers placed on X18 and X19 and no additional peripherals.
Image: qt5-image-demo-mainlinestm32mp1-20200319111217.rootfs.wic.xz
Measured at X43 of PDK2 after system boot and user log in, without any additional scripts. Average current consumption during 30 seconds.
[10] Test condition „stress test": DHCOM STM32MP1 (587-100) variant HS00014 (with WiFi/Bluetooth module and two Ethernet Phys) inside PDK2 (516-400) with all jumpers placed on X18 and X19 and additional Display (560-200)
Image: qt5-image-demo-mainlinestm32mp1-20200319111217.rootfs.wic.xz
Measured at X43 of PDK2 after system boot and user log in. Testskripts: #stress-ng --cpu 2 & #glmark2-es2-drm. Average and maximum current consumption after one complete run of glmark2.

The typical values of the Power consumption vary between different modules, temperatures, the CPU load as well as external devices connected to the DHCOM module.

## 10.3 Reset Timings

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESET_IN | System Reset input assertion time (active low) | 10 | | | ms |
| RESET_OUT | System Reset output assertion time (active low) | 10 | | | ms |

*Table 41: Reset Timings*

## 10.4 Dimensions

**Notes:**

- Figure 10 shows an example with 5,2mm SODIMM-200 socket height.

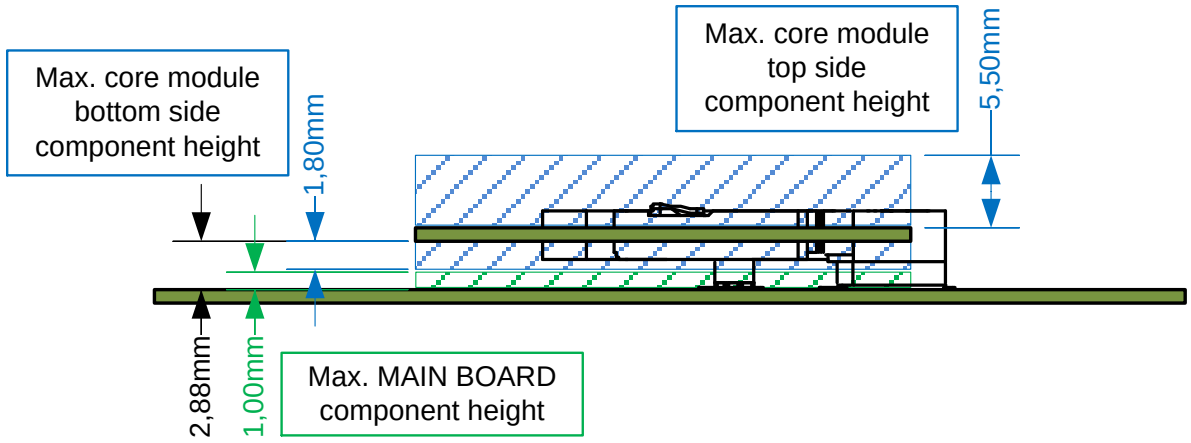


*Figure 10: Maximum component heights*

## 10.4.1 Without DHCOM-X connector

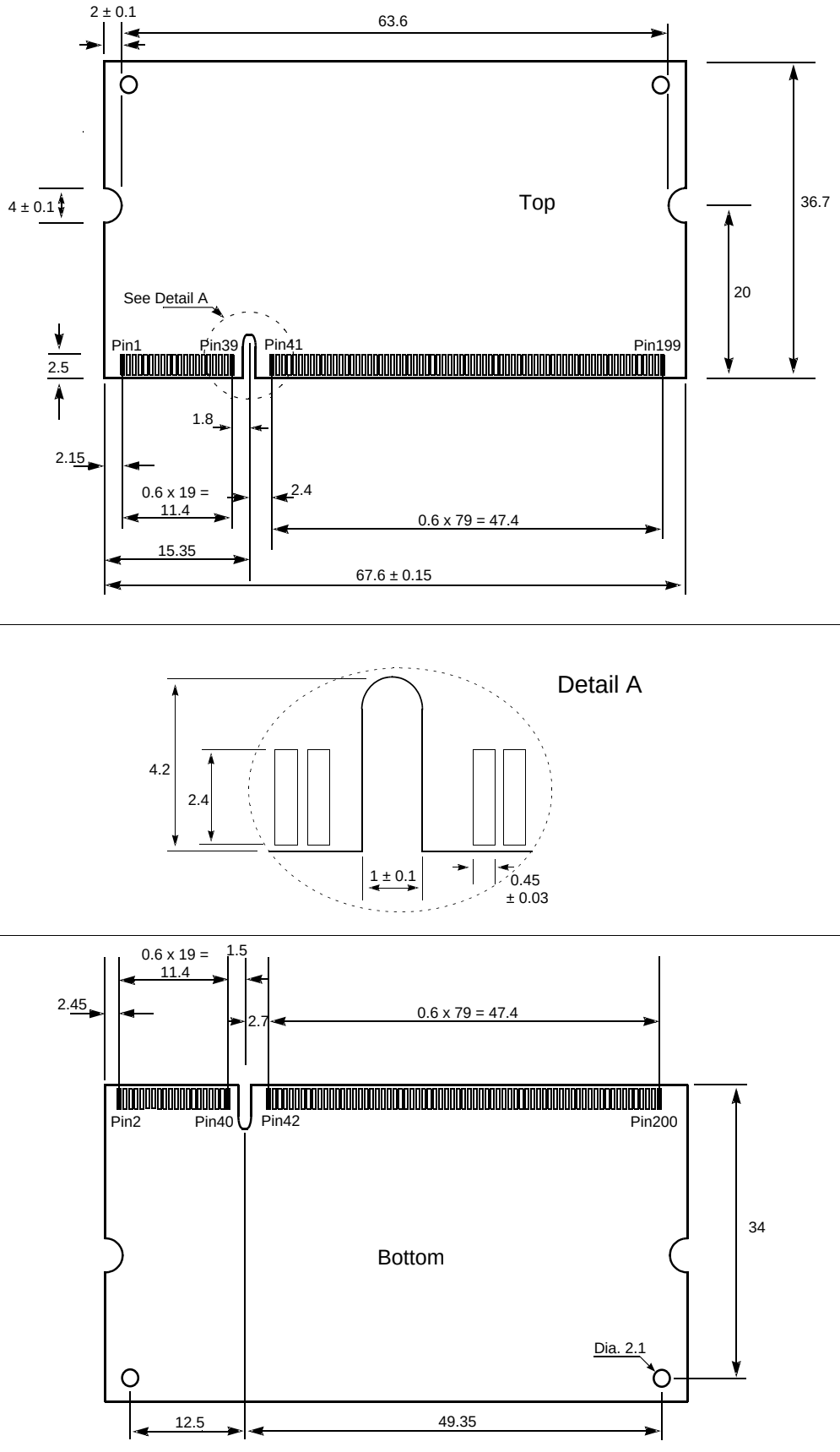


*Figure 11: Dimensions of the DHCOM Module without the DHCOM-X connector*

## 10.4.2 With DHCOM-X connector

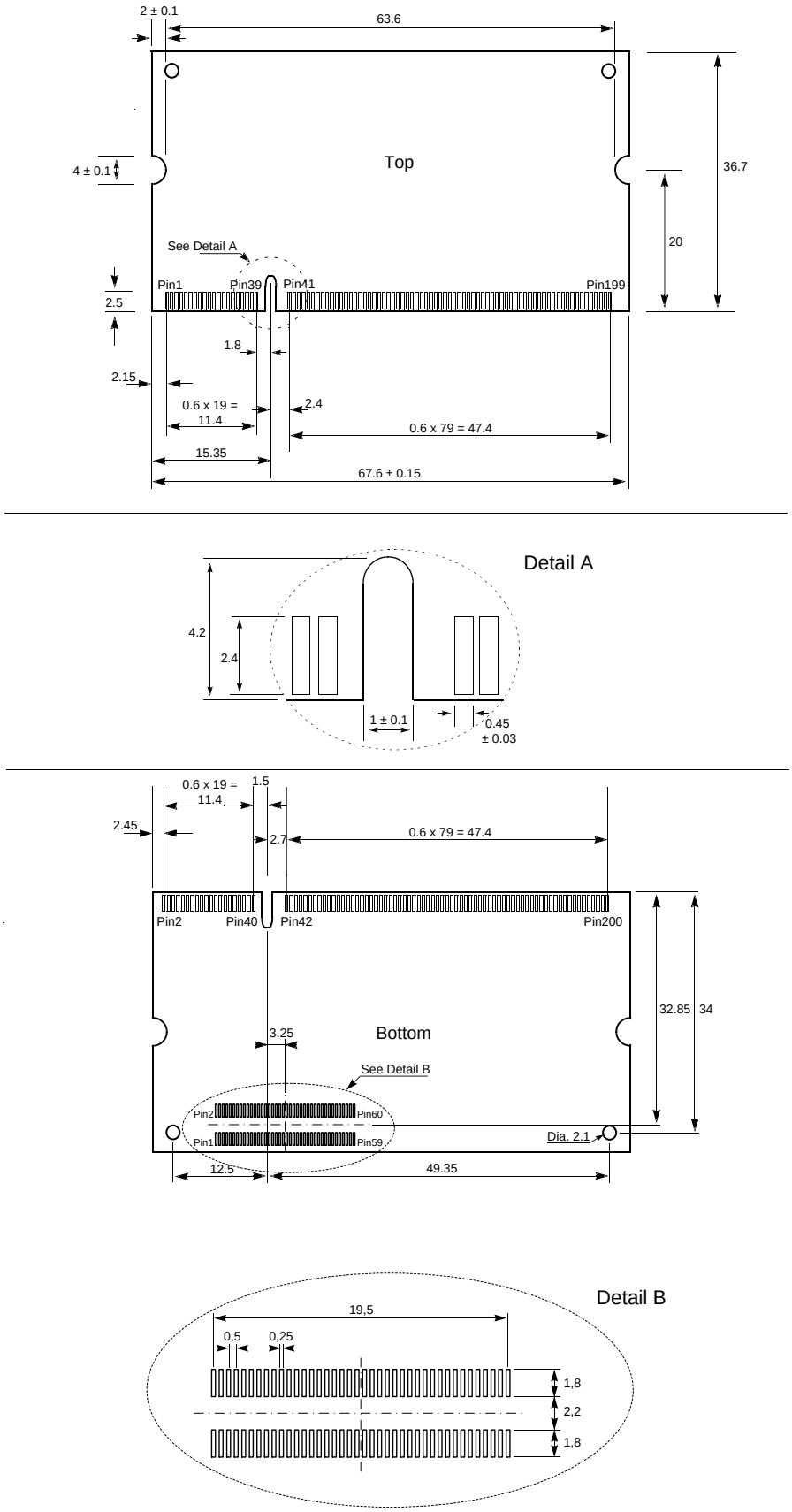


*Figure 12: Dimensions of the DHCOM Module with the DHCOM-X connector*

# 10.5 Mechanical system

Several suggestions are given for the plugs, sockets and cables in the following subsections.

## 10.5.1 SODIMM-200 socket

The DHCM-iMX6UL(L)-01D2 module is designed for operation in a standard 2.5V (DDR) SODIMM-200 memory socket.
The following sockets have been successfully tested with the module:

| Manufacturer | Description | Article number |
|---|---|---|
| **Nexus Components** https://www.nexus-de.com/en | Plug height: 5.2 mm<br>Max. main board component height below the module: 1.0 mm | 5214HB52 |
| **E-tec Interconnect** https://www.e-tec.com/v5/ | Plug height: 5.2 mm<br>Max. main board component height below the module: 1.0 mm | DMD-200-RSE9-55 |
| **Tyco Electronics** https://www.te.com/ | Plug height: 5.2 mm<br>Max. main board component height below the module: 1.0 mm | 1473005-1 |
| **Nexus Components** https://www.nexus-de.com/en | Plug height: 9.2 mm<br>Max. main board component height below the module: 5.0 mm | 5214HB92 |
| **E-tec Interconnect** https://www.e-tec.com/v5/ | Plug height: 9.2 mm<br>Max. main board component height below the module: 5.0 mm | DMD-200-RPE9-55 |
| **Tyco Electronics** https://www.te.com/ | Plug height: 9.2 mm<br>Max. main board component height below the module: 5.0 mm | 1612618-1 |

*Figure 13: SODIMM-200 sockets*

## 10.5.2 DHCOM-X connector

A Molex (https://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector.

DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

| SODIMM-200 socket height | Description | Article number |
|---|---|---|
| **5.2 mm** | 0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits | Molex<br>53748-0808 |
| **9.2 mm** | Not available | Not available |

*Figure 14: DHCOM-X sockets*

## 10.5.3 JTAG and SWD FFC cable

| Manufacturer | Description | Article number |
|---|---|---|
| **Würth Elektronik** https://www.we-online.com/ | 0.50 mm flat flexible cable Type 1 WR-FPC | 687 610 050 002 |
| **Molex** https://www.molex.com/ | 0.50 mm flat flexible cable Type A | 982660097 |

*Figure 15: FFC Cable*

### 10.5.4 JTAG and SWD Tag-Connect cable

| Manufacturer | Description | Article number |
|---|---|---|
| **Tag-Connect**<br>https://www.tag-connect.com/ | 10 pin No-Legs Tag-Connect cable | TC2050-IDC-NL |

## 10.6 Temperature range

| Symbol | Operating temperature range | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T_AMB | Standard configuration | -25 | | 85 | °C |
| T_AMB | On request | -40 | | 85 | °C |

*Figure 16: Temperature range*

# 11 RoHS conformance

This device has been manufactured RoHS II-compliant.