User Manual

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DHCOM iMX25 Module

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Created by AG

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Changes

Version	Date	Changes	State	Name	Notes
1.1	07.04.2011	Manual refers to schematic version 1.4	released	AG	
1.2	12.04.2011	Removed FCI from SODIMM second source connector	released	AG	
1.3	20.04.2011	Added system voltage values to electrical specifications	released	AG	
1.4	26.04.2011	Added processor type and corrected DDR2 clock frequency	released	AG	
1.5	12.05.2011	Added Vbat details	released	AG	
1.6	13.05.2011	Added SODIMM connector to second source supplier	released	AG	
1.7	01.06.2011	Added GPIO requirements	released	AG	
1.8	12.07.2011	• Corrected UART3_RX and TX pin numbers corrected • Adjusted Vbat voltage range • Changed EEPROM size in module block diagram from 1Kbyte to 1Kbit • Changed USB_PWR_STAT and	released	AG	

Version	Date	Changes	State	Name	Notes
		USB_PWR_EN descriptions			
1.9	26.07.2011	Extended DHCOM GPIO requirements	released	AG	
1.10	17.08.2011	• Corrected SPI clock rate • Added SODIMM connector • JTAG adapter • Added 12bit resolution to analog inputs • USB OTG description • Renamed description of LCD contrast to LCD brightness • Added picture of internal core module GPIO circuit	released	AG	
1.11	13.09.2011	Added new picture on page 1	released	SD	
1.12	18.11.2011	• What should be done with “unused” pins? (see Table 1 – Table 21) • Ethernet LED sample circuit (see 3.3) • SD card detection pin is active high (see Table 19) • INT_HIGHEST_PRIORITY pin is active low (see Table 21) • Gold Cap circuit has changed (see Figure 2)	released	AG	

Version	Date	Changes	State	Name	Notes
		• Which pins could be used as a backlight enable GPIO? (see 3.11)			
1.13	16.01.2012	• Added mechanical tolerances (see 6.2) • Added EMI measurements (see 5.0) • Added max. current for output voltages (see 6.1) • Changed max. core module top side component height from 3.0mm to 5.5mm (see 6.2) • Max. SD/MMC interface trace length (see 3.13) • Added hardware design notes. (see 3.) • DHCOM hardware compatibility (see 3.)	released	AG	
1.14	26.03.2012	• DHCOM SPI1_CS0 is now connected to i.MX25 gpio1_GPIO[16] instead of gpio1_GPIO[17] (see 3.6) • DHCOM UART1_CTS is now connected to gpio4GPIO[28] and UART1_RTS to gpio4GPIO[29] (see 3.5.1) • Corrected UART max. baud rate (see 3.5) • Updated hardware overview picture (see 2.0) • Updated function group concept picture	released	AG	

Version	Date	Changes	State	Name	Notes
		(see 3.0) • Added “active low” information for USB Host pins USB_PWR_STAT and USB_PWR_EN (see 3.4.1) • Added USB OTG “enable” and “over current” note (see 3.4.2) • Adapt power consumption and operation current (see 6.1) • Added “active low” information to Reset_In and Reset_Out (see 3.1)			
1.15	30.03.2012	• Added “DHCOM compatibility problem” note with 5 wire touch (see 3.2) • Moved “connection to the DHCOM UART1” note from 3.0 to 3.5.1 • Added “DHCOM compatibility problem” note with SSI interface (see 3.9) • Added trademark sign to I2C • Replaced “not connected” with “reserved” (see Table 22) • Changed “Electrical” to “Electrical - Absolute Maximum Ratings” (see 6.1)	released	AG	
1.16	15.11.2012	• Added ethernet LED pin “not used” information (see 3.3)	released	AG	

Version	Date	Changes	State	Name	Notes
		• Add onboard I²C component addresses (see 3.7) • Supply voltage tolerance has changed (see 6.1) • Add ETH_VIO_SWITCHED absolute maximum ratings (see 6.1) • Updated dimensions figure (see 6.2)			
1.17	26.05.2014	• Add RoHS conformance information	released	AG	
1.18	11.08.2015	• Changed LC_EN description form “LCD display enable” to “LCD display data enable”(see 3.11) • Add power consumption information (see 6.1)	released	AG	

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1 Introduction

1.1 Hardware

The DHCOM iMX25 module is a SODIMM-200 sized computer module based on the Freescale i.MX255 processor. The CPU runs at up to 400 MHz with low power consumption.

It provides all the necessary interfaces for modern embedded devices. The core module contains internal Flash memory and SDRAM. Additionally there are a number of other interfaces available for data storage: USB Memory Stick and SD Card. The module facilitates the connection to passive and active LCDs with resolutions of up to 800x600 pixel, as well as 4/5 wire resistive touch screens. The core module can also be directly connected to a CMOS camera sensor and offers a 10/100 Mbit Ethernet connection as well as a USB host and USB device interface.

1.2 Software

The DHCOM iMX25 module is currently available with the operation systems Windows Embedded CE 6.0 and Embedded Linux. The image contains all necessary drivers for the most common interfaces. A BSP is also available for the module. So the customer is given the option of building his own Windows CE or Linux images.

1.3 Features Overview

- Freescale i.MX255 ARM9 CPU @ 400MHz
- 0 - 2048 MByte NAND flash memory (8bit bus width)
- optional 4MB SPI flash available
- 64 - 128 MByte DDR2-266
- Onboard MicroSD card connector
- SD/MMC card interface, 4bit SDIO
- LC display controller, 16bit colors, 800 x 600 pixel
- Onboard touch controller for 4 (optionally 5 wire resistive touch screens)
- Ethernet controller100/10Mbit

- USB host full-speed
- USB OTG high-speed
- Serial interfaces: 1 x full function UART, 2 x standard UART, 2 x I2C™, 2 x SPI
- CAN interface
- Real time clock module (I2C™ bus interface)
- 1Kbit EEPROM
- 16bit bus interface on SODIMM-200 connector
- 4 x 12bit analog inputs
- JTAG debug connection via FFC connector
- SDIO switch for switching between MicroSD und external SD/MMC connector
- Industrial temperature range (-40°C to 85°C)
- SODIMM-200 connector with DHCOM pin assignment

1.4 Technical manufacturer information

For detailed technical information, refer to the manufacturer websites listed below:

1.4.1 Freescale i.MX25 Processor

Datasheets and technical documents are available on the following website:

http://www.freescale.com

1.4.2 Ethernet PHY LAN8710Ai

Datasheets and technical documents are available on the following website: http://www.smsc.com

1.4.3 Real Time Clock MCP79411T-I/MS

Datasheets and technical documents are available on the following website:

http://www.microchip.com

2 Hardware Overview

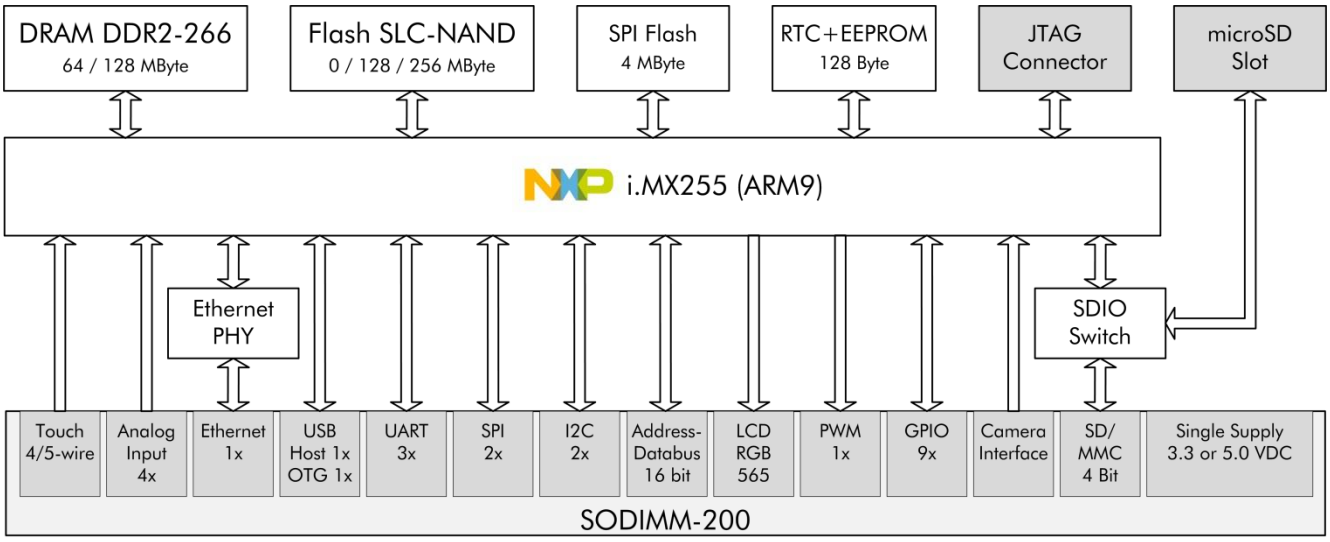


Figure 1: DHCOM iMX25 Module Block Diagram

Figure 1 shows an overview of the DHCOM iMX25 Module components. All the interfaces and memory components are shown in this figure.

3 Signal Description

This chapter describes the signals on the SODIMM-200 connector.

General Notes:

- If a SODIMM-200 pin is not dedicated, the GPIO number is specified. If the GPIO doesn't exist for this pin, the case pin number is specified.
- We recommend pull-up and pull-down resistors with 10k Ohm.

DHCOM hardware compatibility:

The DHCOM Spec. offers function groups to ensure compatibility between different DHCOM core modules. Each function group has its own voltage level output pin (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). A level-shifter on the custom carrier board provides compatibility between different DHCOM core modules. It is possible to omit the level-shifters. In this case DHCOM compatibility is lost.

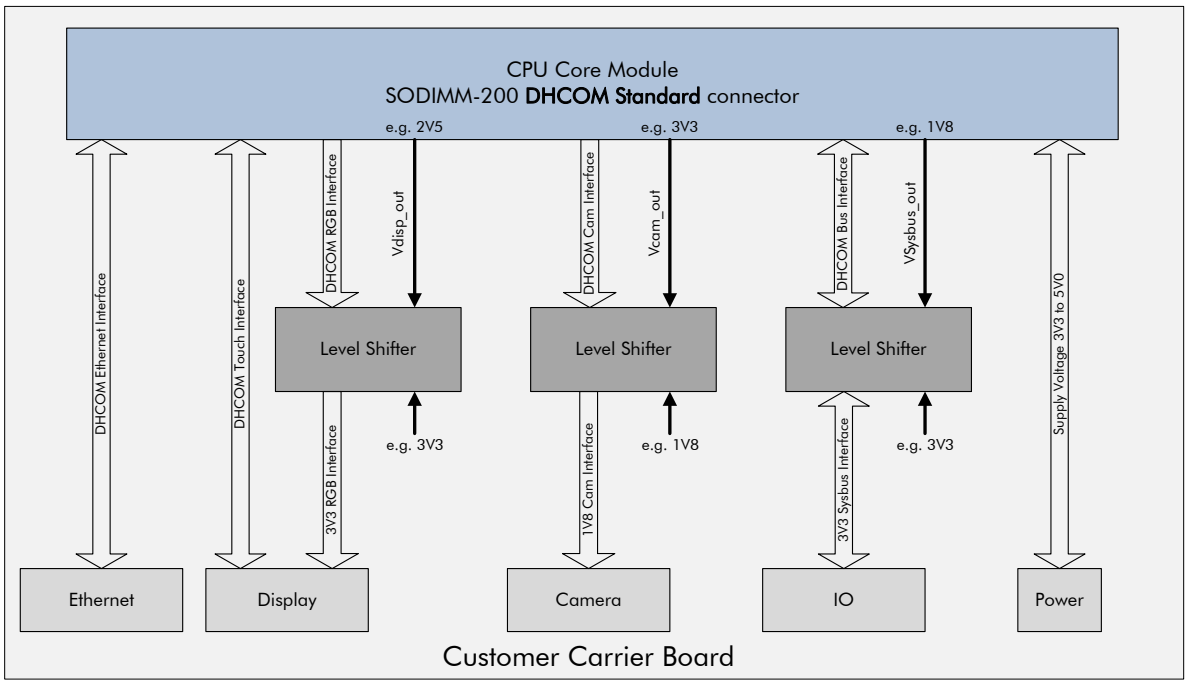


Figure 2: Function Group Concept

3.1 Power Supply & Reset

The DHCOM iMX25 Module works with the following power domains:

- Vin = Core module supply voltage
- Vbat = Battery voltage
- Vsysbus = System bus voltage
- Vdisp = Display voltage
- Vcam = Camera voltage
- VIO = I/O voltage

Important: Connect Vbat to 3,3V, if it is not already connected to a battery or a Gold Cap. Do not leave Vbat unconnected.

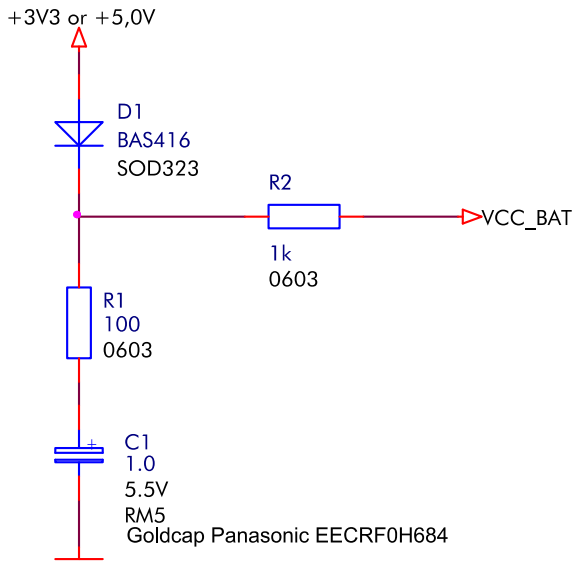


Figure 3: Vbat Gold Cap Example

The SODIMM-200 pins Vsysbus_OUT, Vdisp_OUT, Vcam_OUT and VIO_OUT should be used to detect the supply voltage of the power domain outside the core module.

The SODIMM-200 pin assignment to the power domain is listed in Table 22.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
VCC_IN1	Core module supply voltage input	38	PWR_I	Dedicated pin	MBC
VCC_IN2	Core module supply voltage input	39	PWR_I	Dedicated pin	MBC
VCC_IN3	Core module supply voltage input	40	PWR_I	Dedicated pin	MBC
VCC_IN4	Core module supply voltage input	41	PWR_I	Dedicated pin	MBC
VCC_IN5	Core module supply voltage input	42	PWR_I	Dedicated pin	MBC
VCC_IN6	Core module supply voltage input	44	PWR_I	Dedicated pin	MBC
GND1	Core module ground	17	PWR_I	Dedicated pin	MBC
GND2	Core module ground	19	PWR_I	Dedicated pin	MBC
GND3	Core module ground	43	PWR_I	Dedicated pin	MBC
GND4	Core module ground	45	PWR_I	Dedicated pin	MBC
GND5	Core module ground	47	PWR_I	Dedicated pin	MBC
GND6	Core module ground	101	PWR_I	Dedicated pin	MBC
GND7	Core module ground	111	PWR_I	Dedicated pin	MBC
GND8	Core module ground	153	PWR_I	Dedicated pin	MBC
GND9	Core module ground	185	PWR_I	Dedicated pin	MBC
GND10	Core module ground	199	PWR_I	Dedicated pin	MBC
VCC_BAT	Core module battery voltage input	200	PWR_I	Dedicated pin	MBC
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	Dedicated pin	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	Dedicated pin	-

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
Vcam_OUT	Camera supply voltage output	102	PWR_O	Dedicated pin	-
VIO_OUT	I/O supply voltage output	152	PWR_O	Dedicated pin	-
RESET_IN	System reset input (active low)	21	I	Dedicated pin	-
RESET_OUT	System reset output (active low)	20	O	Dedicated pin	-

Table 1: Power Supply and Reset

3.2 Touch Controller / Analog inputs

The i.MX25 touch screen controller and analog-to-digital converter provide a low-cost resistive touch screen solution. The SODIMM Module can be connected directly to a 4-wire touch panel. 5-wire touch is also possible, but in this case DHCOM compatibility is lost. The i.MX25 also offers up to four auxiliary ADC inputs for analog measurements such as temperature and light or to monitor the battery voltage in portable systems. For detailed information on the touch controller, refer to the Freescale documentation.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
TSPX	Res. touch: 4 wire (X +) / 5 wire (top left)	12	AINOUT	Dedicated pin	PD
TSMX	Res. touch: 4 wire (X -) / 5 wire (top right)	14	AINOUT	Dedicated pin	PD
TSMY	Res. touch: 4 wire (Y -) / 5 wire (bottom right)	16	AINOUT	Dedicated pin	PD
TSPY	Res. touch: 4 wire (Y +) / 5 wire (bottom left)	18	AINOUT	Dedicated pin	PD
Wiper	5 wire res. touch (wiper) (Note: DHCOM compatibility is lost with 5-wire touch)	2	AINOUT	Shared with AD3	PD

Table 2: Resistive Touch

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
AD0	12bit analog input 0	8	AIN	Dedicated pin	PD
AD1	12bit analog input 1	6	AIN	Dedicated pin	PD
AD2	12bit analog input 2	4	AIN	Dedicated pin	PD
AD3	12bit analog input 3	2	AIN	Shared with wiper	PD

Table 3: Analog Inputs

Note: The DHCOM compatibility is lost, if 5 wire touch with wiper pin is used.

3.3 Ethernet

The i.MX25 includes a 10/100 Ethernet MAC and the DHCOM iMX25 module extends its functions by adding a SMSC LAN8710Ai Ethernet PHY. The Ethernet interface is compliant with the IEEE 802.3-2005 standards. For detailed information on the MAC, refer to the Freescale documentation.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
nETH1_LINK_AKT	Port 1: Activity LED connection	186	O	Dedicated pin	PD
nETH1_SPEED100	Port 1: Speed LED connection	188	O	Dedicated pin	PU
ETH1_TXD-	Port 1: Ethernet TX differential output (minus)	190	O	Dedicated pin	PD
ETH1_TXD+	Port 1: Ethernet TX differential output (plus)	192	O	Dedicated pin	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	Dedicated pin	-
ETH1_RXI-	Port 1: Ethernet TX differential input (minus)	196	I	Dedicated pin	PD
ETH1_RXI+	Port 1: Ethernet TX differential input (plus)	198	I	Dedicated pin	PD

Table 4: Ethernet

Note: The LED circuit requires careful attention. Note the following example:

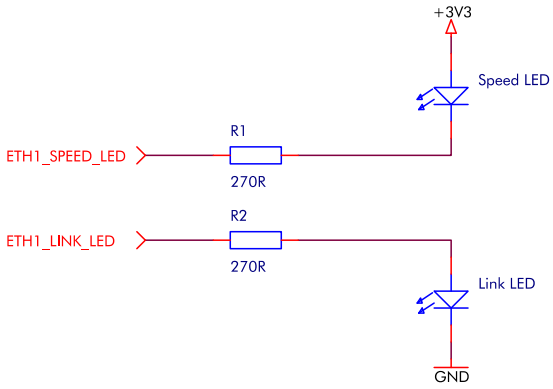


Figure 4: Ethernet LED Circuit

Description: The Ethernet onboard PHY LED pins are also used as configuration straps.

3.4 USB

The i.MX25 includes two USB ports and two on-board PHYs. One port provides On-The-Go (OTG) functionality and can be configured as a host or function port. The second port is a host only port. For detailed information on the USB functionality, refer to the Freescale documentation.

3.4.1 Host

The USB Host port is USB 2.0 compliant but the on-board PHY only supports full-speed operation.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
USB_PWR_STAT	USB host over current indicator (active low)	174	I	gpio1GPIO[26]	-
USB_PWR_EN	USB host power enable signal (active low)	176	O	gpio3GPIO[15]	-
USB_HOST_D1+	USB host differential signal positive line	178	IO	Dedicated pin	PD
USB_HOST_D1-	USB host differential signal negative line	180	IO	Dedicated pin	PD

Table 5: USB Host

3.4.2 OTG

The USB OTG port is USB 2.0 compliant and the on-board PHY supports high-speed operation.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
USB_OTG_VBUS	OTG client: VBUS input line OTG host: USB bus supply voltage	166	I / PWR_O	Dedicated pin	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	Dedicated pin	-
USB_OTG_D+	USB OTG differential signal positive line	170	IO	Dedicated pin	PD
USB_OTG_D-	USB OTG differential signal negative line	172	IO	Dedicated pin	PD

Table 6: USB OTG

Note: The DHCOM USB OTG port do not provide “enable” and “over current” signals. To enable VBUS please use the USB cable ID pin. For monitoring over current, it is possible to connect the USB power management IC over current output to a DHCOM GPIO.

USB On-The-Go Description: A standard USB uses a master/slave architecture; a USB host acts as the protocol master, and a USB 'device' acts as the slave. Only the host can schedule the configuration and data transfers via the link. The devices cannot initiate data transfers, they only respond to requests given by a host.

OTG introduces the concept that a 'device' can perform both the master and slave roles, and so subtly changes the terminology. With OTG, a 'device' can be either a 'host' (acting as the link master) or a 'peripheral' (acting as the link slave). The Device connected to the 'A' end of the cable at start-up (known as the A-device) acts as the default host, while the 'B' end acts as the default peripheral (known as the B-device).

USB On-The-Go does not rule out using a USB hub, but it describes host/peripheral role swapping only in the case of a one-to-one connection where two OTG devices are directly connected. Role swapping does not work through a standard hub, as one device will act as the host and the other as the peripheral until they are disconnected.

The original USB On-The-Go standard introduces a plug receptacle called mini-AB. It accepts either a mini-A plug or a mini-B plug. The standard OTG cable has a mini-A plug on one side and a mini-B plug on the other (it could not have two plugs of the same type). The device with the mini-A plug becomes an OTG A-device, and the one with the mini-B plug becomes a B-device. The type of plug inserted is detected by the status of the pin ID (the mini-A plug has the ID pin grounded while the ID in the mini-B plug is floating).

Pure Mini-A plugs are also available for use when only a host port is required.

USB OTG must supply a minimum current of 8mA but it could also provide up to 500mA, like a normal USB.

3.5 UART

The DHCOM iMX25 Module offers three OnChip UARTs. All three ports are high-speed TIA/EIA-232-F compatible and permit maximum a baud rate of 4.15 Mbit/s. For detailed information on the UART functionality, refer to the Freescale documentation.

3.5.1 Full Function UART

The first UART is a full function UART which supports modem-control capability.

Note: The UART uses i.MX25 instance UART2.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
UART1_DTR	Full function UART data terminal ready	22	O	gpio4GPIO[22]	-
UART1_CTS	Full function UART clear to send	24	I	gpio4GPIO[28]	-
UART1_RTS	Full function UART request to send	26	O	gpio4GPIO[29]	-
UART1_DSR	Full function UART data set ready	28	I	gpio4GPIO[23]	-
UART1_DCD	Full function UART data carrier detect	30	I	gpio4GPIO[24]	-
UART1_RX	Full function UART receive data line	32	I	gpio4GPIO[26]	-
UART1_TX	Full function UART transmit data line	34	O	gpio4GPIO[27]	-
UART1_RI	Full function UART ring indicator	36	I	gpio4GPIO[25]	-

Table 7: Full Function UART 1

Hardware Design Note:

It is necessary to provide a connection to the DHCOM UART1, as the core module bootloader could be controlled via the UART1. A minimum connection level should be provided via solder pads.

3.5.2 Standard UART with CTS and RTS

The second UART does not support modem-control capability, but it offers two GPIOs which can be used to generate RTS and CTS signals with software.

Note: The UART uses i.MX25 instance UART3.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
UART2_CTS	GPIO to generate software controller CTS	31	I	gpio2GPIO[15]	-
UART2_RTS	GPIO to generate software controller RTS	33	O	gpio2GPIO[10]	-
UART2_RX	Bluetooth UART receive data line	35	I	gpio2GPIO[29]	-
UART2_TX	Bluetooth UART transmit data line	37	O	gpio2GPIO[30]	-

Table 8: Standard UART 2

3.5.3 Standard UART

The third UART does not support modem-control capability.

Note: The UART uses i.MX25 instance UART5.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
UART3_RX	Serial port receive data line	23	I	gpio3GPIO[24]	-
UART3_TX	Serial port transmit data line	25	O	gpio3GPIO[23]	-

Table 9: Standard UART

3.6 Synchronous Serial Port

The DHCOM iMX25 module offers two CSPI (configurable serial peripheral interface) ports. The CSPI module is a full-duplex, synchronous, four-wire serial communication module and provides the following features:

- Master/slave configurable
- Full-duplex synchronous serial interface
- Transfer continuation function allows unlimited length data transfers

- 32-bit wide by 8-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Max operation frequency up to 16,625MHz

For detailed information on the CSPI functionality, refer to the Freescale documentation.

Note: The SPI Port 1 uses i.MX25 instance CSPI1.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
SPI1_CS0	Slave select signal	177	IO	gpio1GPIO[16]	-
SPI1_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	gpio1GPIO[18]	-
SPI1_MISO	SSP receive data line	181	I	gpio1GPIO[15]	-
SPI1_MOSI	SSP transmit data line	183	O	gpio1GPIO[14]	-

Table 10: SPI Port 1

Note: The SPI port 2 uses i.MX25 instance CSPI3.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
SPI2_CS0	Slave select signal (only if camera interface is not used)	155	IO	gpio1GPIO[31]	-
SPI2_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation) (only if camera interface is not used)	157	IO	gpio1GPIO[29]	-
SPI2_MISO	SSP receive data line (only if camera interface is not used)	159	I	gpio1GPIO[28]	-
SPI2_MOSI	SSP transmit data line (only if camera interface is not used)	161	O	gpio1GPIO[27]	-

Table 11: SPI Port 2

3.7 I²C

The DHCOM iMX25 module has two I2C™ Ports. The interface is a true multi-master bus including collision detection and arbitration. It supports standard-speed (100kbps) and fast-mode (400kbps) operation. For the I²C bus specification, refer to the Philips semiconductor I²C Bus specification.

Pull-up resistors, required by the I²C-Spec. have also been added onboard.

Notes:

- The I²C port 1 uses i.MX25 instance I2C1.
- The following components are connected to DHCOM I²C port 1:
  - RTC EEPROM (7bit address: 0x57)
  - RTC (7bit address: 0x6F)

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
I2C1_CLK	I²C clock line	182	IO	gpio1GPIO[12]	-
I2C1_DATA	I²C data line	184	IO	gpio1GPIO[13]	-

Table 12: I²C Port 1

Note: The I²C port 2 uses i.MX25 instance I2C2.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
I2C2_CLK	I²C clock line	158	IO	gpio1GPIO[2]	-
I2C2_DATA	I²C data line	160	IO	gpio1GPIO[3]	-

Table 13: I²C Port 2

3.8 CAN

The i.MX25 FlexCAN module is a communication controller that implements the CAN protocol according to the CAN 2.0B protocol specification. This specification supports both standard and extended message frames. For detailed information on CAN functionality, refer to the Freescale documentation.

Note: The CAN port uses i.MX25 instance CAN1.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
CAN_TX	CAN transmit data line	27	IO	gpio1GPIO[0]	-
CAN_RX	CAN receive data line	29	IO	gpio1GPIO[1]	-

Table 14: CAN Port

3.9 SSI and AUDMUX

Note: The SSI interface is only available on the SODIMM-200 with a special customer variant of the DHCOM iMX25 module. If the customer uses the SSI interface, the DHCOM compatibility is lost.

The synchronous serial interface is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices. These serial devices can be standard CODer-DECoder (CODECs), digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio CODECs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.

The digital audio mux (AUDMUX) provides a programmable interconnected device for voice, audio, and synchronous data routing between host serial interfaces (such as SSI) and peripheral serial interfaces (that is, audio and voice CODECs, also known as coder-decoders). The AUDMUX interconnections allow multiple, simultaneous, audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations.

For detailed information on the SSI and AUDMUX functionality, refer to the Freescale documentation.

Note: The SSI Port uses i.MX25 instance AUDMUX Port 5.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
I2S_RXFS	Receive frame sync input/output	1	IO	gpio3GPIO[0]	-
I2S_RXD	Receive data	5	I	gpio3GPIO[2]	-
I2S_RXC	Receive clock input/output	7	IO	gpio2GPIO[31]	-
I2S_TXFS	Transmit frame sync input/output	11	IO	gpio3GPIO[4]	-
I2S_TXC	Transmit clock input/output	13	IO	gpio3GPIO[3]	-
I2S_TXD	Transmit data	15	O	gpio3GPIO[1]	-

Table 15: SSI and AUDMUX Port

3.10 Address- and Data bus

The i.MX25 memory-bus interface is also connected to the SODIMM-200 connector. For specific information, please refer to the Freescale documentation.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	Dedicated pin	-
A00 – A15	Memory controller address line	See 4 Connectors	O	Dedicated pins	-
D00 – D15	Memory controller data line	See 4 Connectors	IO	Dedicated pins	-
CS_A	Static memory chip select 0	128	O	gpio4GPIO[2]	-
CS_B	Static memory chip select 1	129	O	gpio4GPIO[3]	-
CS_C	Static memory chip select 3	130	O	gpio3GPIO[20]	-
CS_D	Static memory chip select 4 (only if module has 64MByte DDR2 SDRAM)	131	O	Dedicated pin	-
WE	Memory controller write enable	133	O	gpio3GPIO[25]	-
OE	Memory controller output enable	134	O	gpio2GPIO[14]	-

Table 16: Address- and Data Bus

3.11 LCD Controller

The DHCOM iMX25 module provides a 16bit (RGB 5:6:5) LCD interface on the SODIMM-200 connector. It can be connected to passive and active LCDs with resolutions of up to 800x600 Pixel.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	Dedicated Pin	-
LC_R3	LCD display data red 0	51	O	contact W4	-
LC_R4	LCD display data red 1	53	O	contact V4	-
LC_R5	LCD display data red 2	55	O	contact W3	-
LC_R6	LCD display data red 3	57	O	gpio1GPIO[4]	-
LC_R7	LCD display data red 4	59	O	gpio1GPIO[5]	-
LC_G2	LCD display data green 0	61	O	gpio1GPIO[20]	-
LC_G3	LCD display data green 1	63	O	gpio1GPIO[21]	-
LC_G4	LCD display data green 2	65	O	contact V6	-
LC_G5	LCD display data green 3	67	O	contact W5	-
LC_G6	LCD display data green 4	69	O	contact Y4	-
LC_G7	LCD display data green 5	71	O	contact Y3	-
LC_B3	LCD display data blue 0	75	O	gpio2GPIO[16]	-
LC_B4	LCD display data blue 1	77	O	gpio2GPIO[17]	-
LC_B5	LCD display data blue 2	79	O	gpio2GPIO[18]	-
LC_B6	LCD display data blue 3	81	O	gpio2GPIO[19]	-
LC_B7	LCD display data blue 4	83	O	gpio1GPIO[19]	-
LC_EN	LCD display data enable	85	O	gpio1GPIO[25]	-
LC_VSYNC	LCD frame or vertical sync. puls	87	O	gpio1GPIO[23]	-
LC_HSYNC	LCD line or horizontal sync. puls	89	O	gpio1GPIO[22]	-

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
LC_PCLK	LCD pixel clock	91	O	gpio1GPIO[24]	-
GPIO_PWM	LCD brightness (only if PWM is not used)	100	O	contact U4	-

Table 17: LCD Controller

Note: Each of the DHCOM GPIO_* pins could be used for backlight control (backlight enable GPIO). The GPIO and the activity (high or low) could be configured via the DHCOM hardware settings block.

3.12 PWM

The DHCOM iMX25 module provides one PWM channel on the SODIMM-200 connector. The i.MX25 PWM channels have a 16-bit resolution and include a FIFO to generate sound. For detailed information on the PWM functionality, refer to the Freescale documentation.

Note: The PWM uses i.MX25 instance PWM4.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
GPIO_PWM	PWM channel (only if LCD brightness is not used)	100	O	contact U4	-

Table 18: PWM

3.13 eSDHC

The i.MX25 eSDHC controller is based on the standards outlined in the following specifications:

- MMC system specification version 4.2
- SD host controller standard specification version 2.0, including test event register support
- SD memory card specification version 2.0 supports high-capacity SD memory cards
- SDIO card specification version 2.0

- CE-ATA card specification version 1.0

The DHCOM iMX25 module provides an onboard MircoSD card. The card is also connected to the i.MX25 eSDHC controller. It is possible to switch between the MicroSD card and an external connected card with the integrated SDIO switch.

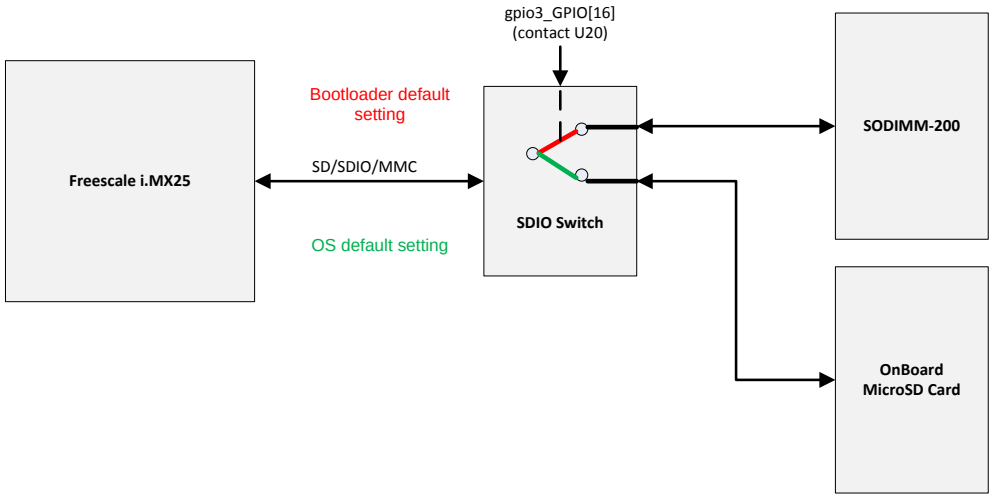


Figure 5: SD/SDIO/MMC Interface Overview

Note: The eSDHC port uses i.MX25 instance eSDHC1.

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	gpio2GPIO[24]	-
SD_CMD	SD/SDIO/MMC command line	104	IO	gpio2GPIO[23]	-
SD_DETECT	SD/SDIO/MMC card detection: active high	105	I	gpio2GPIO[21]	PD
SD_D0	SD/SDIO/MMC data line	106	IO	gpio2GPIO[25]	-
SD_D1	SD/SDIO/MMC data line	107	IO	gpio2GPIO[26]	-
SD_D2	SD/SDIO/MMC data line	108	IO	gpio2GPIO[27]	-
SD_D3	SD/SDIO/MMC data line	109	IO	gpio2GPIO[28]	-

Table 19: SD/SDIO/MMC Interface

Note: The max. trace length from the SODIMM-200 connector to the SD/MMC slot is 80mm. It is necessary to route traces of equal length.

3.14 CMOS Sensor Interface

The CMOS sensor interface facilitates connection to external CMOS image sensors. The DHCOM iMX25 module supports only 8bit connection to the sensors. The CSI interface includes the following capabilities:

- Configurable interface logic to support most commonly available CMOS sensors
- Support for CCIR656 video interface as well as traditional sensor interface
- 8bit data port for YCC, YUV, or RGB data input
- 8bit data port for Bayer data input
- Full control of 8bit/pixel data format to 32bit receive FIFO packing
- 128 × 32 FIFO to store received image pixel data
- Reception FIFO overrun protection mechanism

For detailed information on the CSI functionality, refer to the Freescale documentation.

User Manual

Pin Name	Description	SODIMM Pin Nr.	IO Type	Multiplexed	Not used
Vcam_OUT	Camera supply voltage output	102	PWR_O	Dedicated Pin	-
CIF_D2	CSI Interface data line 2	52	I	gpio1GPIO[27]	-
CIF_D3	CSI Interface data line 3	54	I	gpio1GPIO[28]	-
CIF_D4	CSI Interface data line 4	56	I	gpio1GPIO[29]	-
CIF_D5	CSI Interface data line 5	58	I	gpio1GPIO[30]	-
CIF_D6	CSI Interface data line 6	60	I	gpio1GPIO[31]	-
CIF_D7	CSI Interface data line 7	62	I	gpio1GPIO[6]	-
CIF_D8	CSI Interface data line 8	64	I	gpio1GPIO[7]	-
CIF_D9	CSI Interface data line 9	66	I	gpio4GPIO[21]	-
CIF_VSYNC	CSI Interface frame synchronization	68	IO	gpio1GPIO[8]	-
CIF_MCLK	CSI Interface master clock output	70	O	gpio1GPIO[9]	-
CIF_PCLK	CSI Interface pixel clock input	72	I	gpio1GPIO[11]	-
CIF_HSYNC	CSI Interface line synchronization	74	IO	gpio1GPIO[10]	-

Table 20: CSI Interface

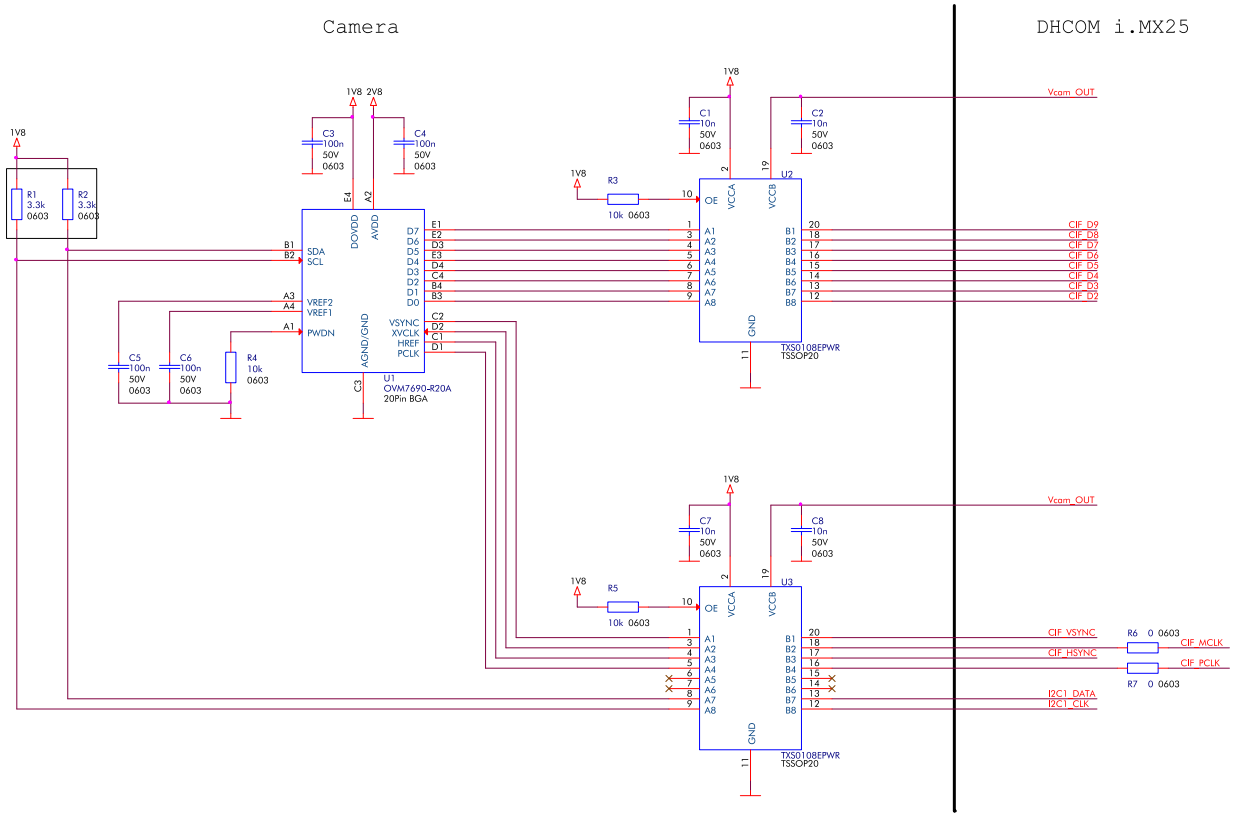


Figure 6: Camera Example

3.15 GPIOs

The i.MX25 provides multiplexed general purpose I/O pins for use in the generation and capturing application of specific input and output signals. Free GPIOs are shown in Table 21. Most of the multiplexed pins can also be used as GPIO, if their allocated function is not in use, but in this case the DHCOM compatibility is lost.

Pin Name	Description	SODIMM Pin Nr.	i.MX25 GPIO Number	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	gpio3GPIO[14]	PU
GPIO _A [1)]	General purpose I/O	154	gpio2GPIO[12]	-
GPIO _B [1)]	General purpose I/O	156	gpio3GPIO[21]	-
GPIO _C [1)]	General purpose I/O	162	gpio2GPIO[4]	-
GPIO _D [1)]	General purpose I/O	163	gpio2GPIO[5]	-
GPIO _E [1)]	General purpose I/O	164	gpio2GPIO[6]	-
GPIO _F [1)]	General purpose I/O	165	gpio2GPIO[7]	-
GPIO _G [1)]	General purpose I/O	167	gpio2GPIO[8]	-
GPIO _H [1)]	General purpose I/O	173	gpio2GPIO[9]	-
GPIO _I	General purpose I/O	175	gpio3GPIO[17]	-

Table 21: GPIOs

1) Used as output: If one of the GPIOs is set to high state, consider that the internal resistance to 3V3 is 4kΩ. If a driven output is required, a buffer must be added, e.g. SN74AHC1G125.

   Or you can use the following transistor circuit:

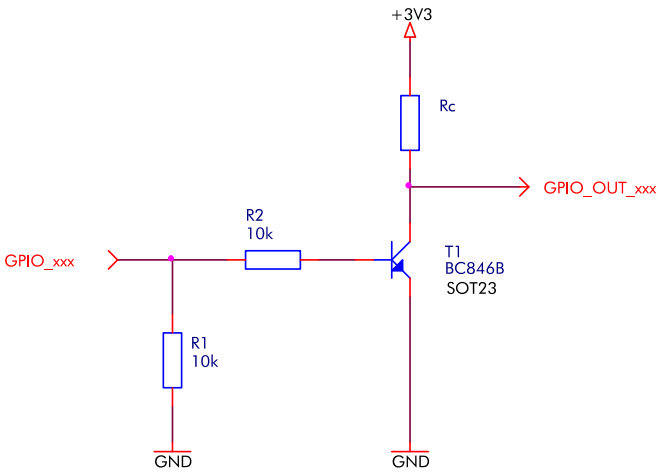


Figure 7: Transistor Example Circuit

Used as Input: If one of the GPIOs is used as input, consider that the driving source needs a drive strength of at least ±2 mA.

Background: GPIO_A up to GPIO_H are realized with 1,8V i.MX25 GPIO pins and bidirectional voltage-level translators to maintain compatibility with the VIO voltage of 3,3V.

For a detailed description of the used level shifters TSX010*E refer to the Texas Instruments homepage: http://www.ti.com

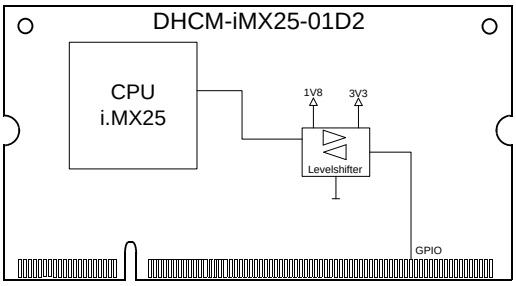


Figure 8: Internal Core Module GPIO Circuit

4 Connectors

Additionally to the SODIMM-200 connector, the DHCOM iMX25 module is equipped with a 10pin FFC JTAG connector.

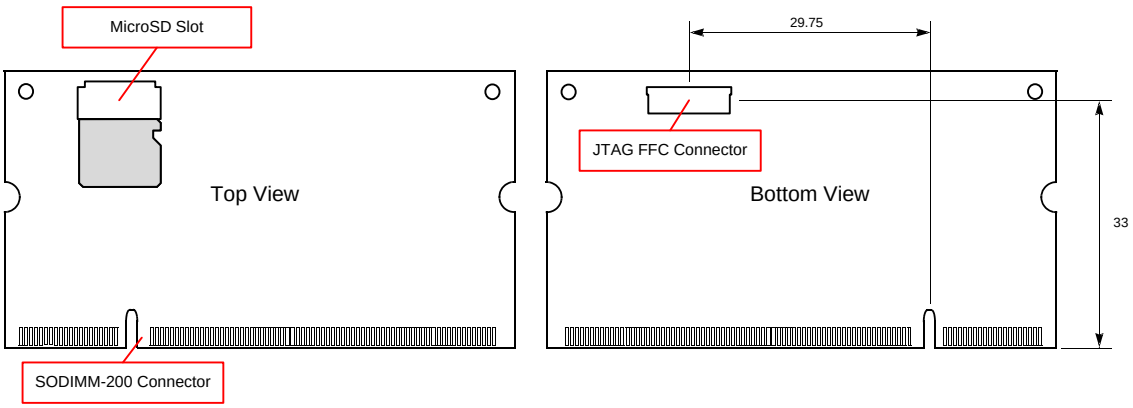


Figure 9: Connectors Location

4.1 SODIMM-200

Pin Number	Pin Name	Power Domain	Pin Number	Pin Name	Power Domain
1	(I2S_RXFS) *Reserved*	VIO	2	AD3	VDDA
3	*Reserved*		4	AD2	VDDA
5	(I2S_RXD) *Reserved*	VIO	6	AD1	VDDA
7	(I2S_RXC) *Reserved*	VIO	8	AD0	VDDA
9	*Reserved*		10	*Reserved*	
11	(I2S_TXFS) *Reserved*	VIO	12	TSPX	VDDA
13	(I2S_TXC) *Reserved*	VIO	14	TSMX	VDDA
15	(I2S_TXD) *Reserved*	VIO	16	TSMY	VDDA
17	GND1	Vin	18	TSPY	VDDA
19	GND2	Vin	20	RESET_OUT	VIO
21	RESET_IN	VIO	22	UART1_DTR	VIO
23	UART3_RX	VIO	24	UART1_CTS	VIO
25	UART3_TX	VIO	26	UART1_RTS	VIO
27	CAN_TX	VIO	28	UART1_DSR	VIO
29	CAN_RX	VIO	30	UART1_DCD	VIO
31	UART2_CTS (Note: only GPIO)	VIO	32	UART1_RX	VIO
33	UART2_RTS (Note: only GPIO)	VIO	34	UART1_TX	VIO
35	UART2_RX	VIO	36	UART1_RI	VIO
37	UART2_TX	VIO	38	VCC_IN1	Vin

Pin Number	Pin Name	Power Domain	Pin Number	Pin Name	Power Domain
39	VCC_IN2	Vin	40	VCC_IN3	Vin
41	VCC_IN4	Vin	42	VCC_IN5	Vin
43	GND3	Vin	44	VCC_IN6	Vin
45	GND4	Vin	46	Vdisp_OUT	Vdisp
47	GND5	Vin	48	*Reserved*	
49	*Reserved (internal PU)*		50	*Reserved*	
51	LC_R3	Vdisp	52	CIF_D2	Vcam
53	LC_R4	Vdisp	54	CIF_D3	Vcam
55	LC_R5	Vdisp	56	CIF_D4	Vcam
57	LC_R6	Vdisp	58	CIF_D5	Vcam
59	LC_R7	Vdisp	60	CIF_D6	Vcam
61	LC_G2	Vdisp	62	CIF_D7	Vcam
63	LC_G3	Vdisp	64	CIF_D8	Vcam
65	LC_G4	Vdisp	66	CIF_D9	Vcam
67	LC_G5	Vdisp	68	CIF_VSYNC	Vcam
69	LC_G6	Vdisp	70	CIF_MCLK	Vcam
71	LC_G7	Vdisp	72	CIF_PCLK	Vcam
73	*Reserved (internal PU)*		74	CIF_HSYNC	Vcam
75	LC_B3	Vdisp	76	*Reserved (internal PU)*	
77	LC_B4	Vdisp	78	*Reserved (internal PU)*	

Pin Number	Pin Name	Power Domain	Pin Number	Pin Name	Power Domain
79	LC_B5	Vdisp	80	*Reserved (internal PU)*	
81	LC_B6	Vdisp	82	*Reserved (internal PU)*	
83	LC_B7	Vdisp	84	*Reserved (internal PU)*	
85	LC_EN	Vdisp	86	*Reserved (internal PU)*	
87	LC_VSYNC	Vdisp	88	*Reserved*	
89	LC_HSYNC	Vdisp	90	*Reserved*	
91	LC_PCLK	Vdisp	92	*Reserved*	
93	*Reserved*		94	*Reserved*	
95	*Reserved*		96	*Reserved*	
97	*Reserved*		98	*Reserved*	
99	*Reserved*		100	GPIO_PWM	VIO
101	GND6	Vin	102	Vcam_OUT	Vcam
103	SD_CLK	VIO	104	SD_CMD	VIO
105	SD_DETECT	VIO	106	SD_D0	VIO
107	SD_D1	VIO	108	SD_D2	VIO
109	SD_D3	VIO	110	Vsysbus_OUT	Vsysbus
111	GND7	Vin	112	A8	Vsysbus
113	A0	Vsysbus	114	A9	Vsysbus
115	A1	Vsysbus	116	A10	Vsysbus
117	A2	Vsysbus	118	A11	Vsysbus

Pin Number	Pin Name	Power Domain	Pin Number	Pin Name	Power Domain
119	A3	Vsysbus	120	A12	Vsysbus
121	A4	Vsysbus	122	A13	Vsysbus
123	A5	Vsysbus	124	A14	Vsysbus
125	A6	Vsysbus	126	A15	Vsysbus
127	A7	Vsysbus	128	CS_A	Vsysbus
129	CS_B	Vsysbus	130	CS_C	Vsysbus
131	*CS_D*	Vsysbus	132	*Reserved (internal PU)*	
133	WE	Vsysbus	134	OE	Vsysbus
135	D0	Vsysbus	136	D8	Vsysbus
137	D1	Vsysbus	138	D9	Vsysbus
139	D2	Vsysbus	140	D10	Vsysbus
141	D3	Vsysbus	142	D11	Vsysbus
143	D4	Vsysbus	144	D12	Vsysbus
145	D5	Vsysbus	146	D13	Vsysbus
147	D6	Vsysbus	148	D14	Vsysbus
149	D7	Vsysbus	150	D15	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO	152	VIO_OUT	VIO
153	GND8	Vin	154	GPIO_A	VIO
155	SPI2_CS0	VIO	156	GPIO_B	VIO
157	SPI2_CLK	VIO	158	I2C2_CLK	VIO

Pin Number	Pin Name	Power Domain
159	SPI2_MISO	VIO
161	SPI2_MOSI	VIO
163	GPIO_D	VIO
165	GPIO_F	VIO
167	GPIO_G	VIO
169	*Reserved*	
171	*Reserved*	
173	GPIO_H	VIO
175	GPIO_I	VIO
177	SPI1_CS0	VIO
179	SPI1_CLK	VIO
181	SPI1_MISO	VIO
183	SPI1_MOSI	VIO
185	GND9	Vin
187	*Reserved*	
189	*Reserved*	
191	*Reserved*	
193	*Reserved*	
195	*Reserved*	
197	*Reserved*	

Pin Number	Pin Name	Power Domain
160	I2C2_DATA	VIO
162	GPIO_C	VIO
164	GPIO_E	VIO
166	USB_OTG_VBUS	VIO
168	USB_OTG_ID	VIO
170	USB_OTG_D+	VIO
172	USB_OTG_D-	VIO
174	USB_PWR_STAT	VIO
176	USB_PWR_EN	VIO
178	USB_HOST_D1+	VIO
180	USB_HOST_D1-	VIO
182	I2C1_CLK	VIO
184	I2C1_DATA	VIO
186	nETH1_LINK_AKT	VIO
188	nETH1_SPEED100	VIO
190	ETH1_TXD-	VIO
192	ETH1_TXD+	VIO
194	ETH_VIO_SWITCHED	VIO
196	ETH1_RXI-	VIO
198	ETH1_RXI+	VIO

Pin Number	Pin Name	Power Domain
199	GND10	Vin

Pin Number	Pin Name	Power Domain
200	VCC_BAT	Vbat

Table 22: SODIMM-200 Assignment

4.2 JTAG

Pin Number	Pin Name
1	+3V3 output
2	GND
3	JTAG_TMS
4	#JTAG_TRST
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	*Reserved (internal PD)*
10	i.MX25 DE_B pad

Table 23: JTAG Connector Assignment

Adapter: The DHCOM evaluation board incorporates an adapter from a 10pin FFC connector to a 20pin standard JTAG debug connector for ARM cores. It is also possible to get a separate adapter to the 20pin standard interface. Please contact DH electronics GmbH for more information.

Debugger Tools: For JTAG Debugger Tools go to http://www.lauterbach.com.

5 EMI - Radio Noise Field Strength

Measured with DHCOM i.MX25 module inserted in DHeva01 board.

5.1 EN55011, Class A, Antenna 1,20m horizontal

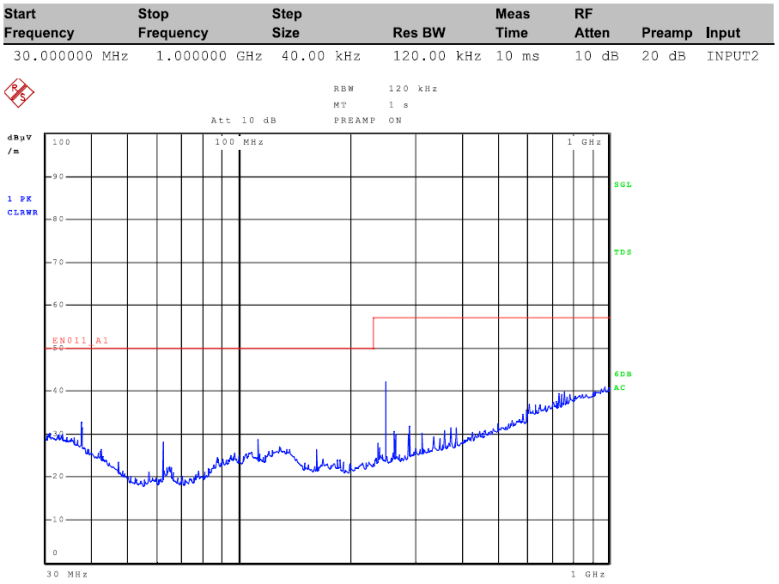


Figure 10: EMI - Antenna 1,20m Horizontal

5.2 EN55011, Class A, Antenna 1,50m vertical

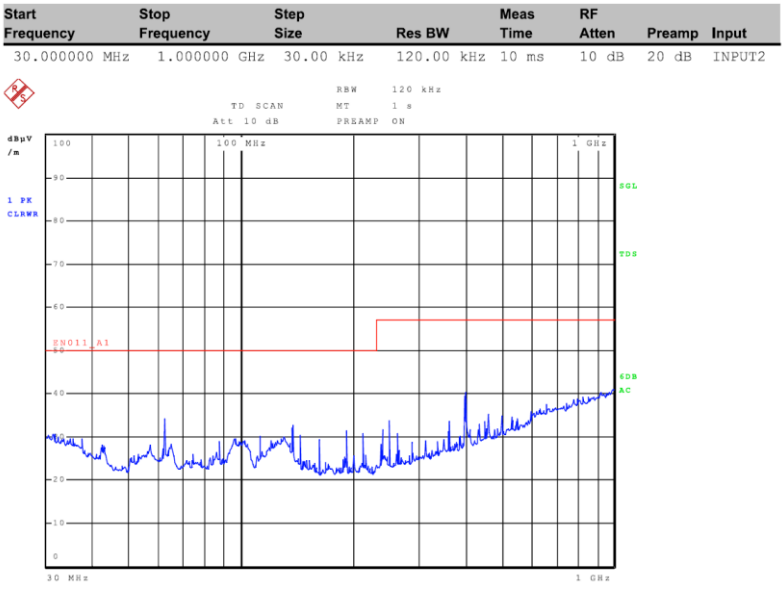


Figure 11: EMI - Antenna 1,50m Vertical

6 Technical Specifications

6.1 Electrical - Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT	3.3	3.3 or 5.0	5.5	V
V_{bat}	Battery voltage INPUT	1.3V		5.5	V
V_{sysbus}	System bus voltage OUTPUT		1.8		V
$I_{Vsysbus}$	Vsysbus current			20	mA
V_{disp}	Display voltage OUTPUT		3.3		V
I_{Vdisp}	Vdisp current			20	mA
V_{cam}	Camera voltage OUTPUT		3.3		V
I_{Vcam}	Vcam current			20	mA
V_{IO}	I/O voltage OUTPUT		3.3		V
I_{VIO}	VIO current			20	mA
$V_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
$I_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED current			60	mA
I_{IN} VCC = 3.3V	Operating current (without V*_OUT pins)		230	410	mA
I_{IN} VCC = 5V	Operating current (without V*_OUT pins)		170	300	mA
Power (Vin) VCC = 3.3V	i.MX25 core module power consumption (without V*_OUT pins)		750	1350	mW
Power (Vin) VCC = 5V	i.MX25 core module power consumption (without V*_OUT pins)		850	1500	mW
I_{Vbat}	Vbat input current			5	mA

Symbol	Description	Min	Typ	Max	Unit
I_{Vbat_Stby}	Vbat Standby input current			700	nA
V_{IH_3V3}	Digital input high voltage	2.52	3.3	3.6	V
V_{IL_3V3}	Digital input low voltage	-0.3	0	0.9	V
V_{IH_1V8}	Digital input high voltage	1.33	1.8	1.9	V
V_{IL_1V8}	Digital input low voltage	-0.3		0.52	V

Table 24: Electrical DC Characteristics

6.2 Dimensions

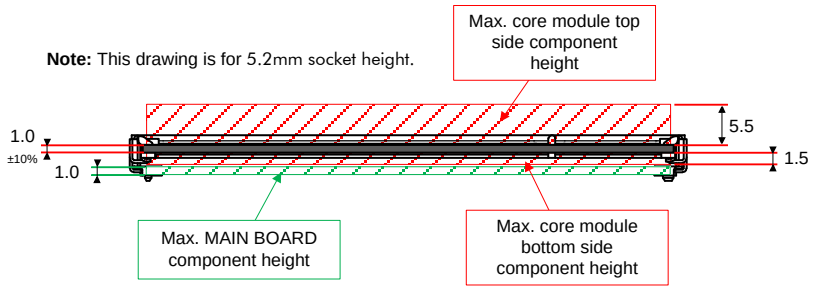
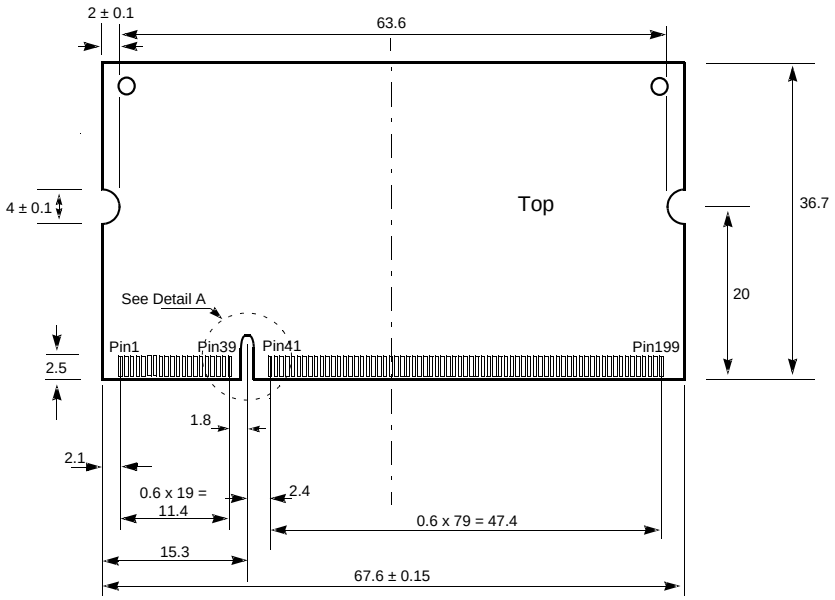
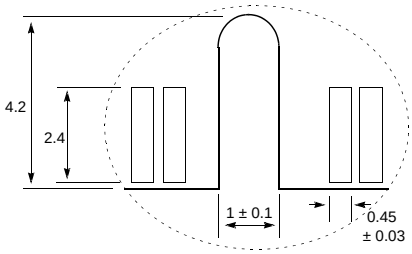


Figure 12: Component Height

Note: All dimensions are in mm.





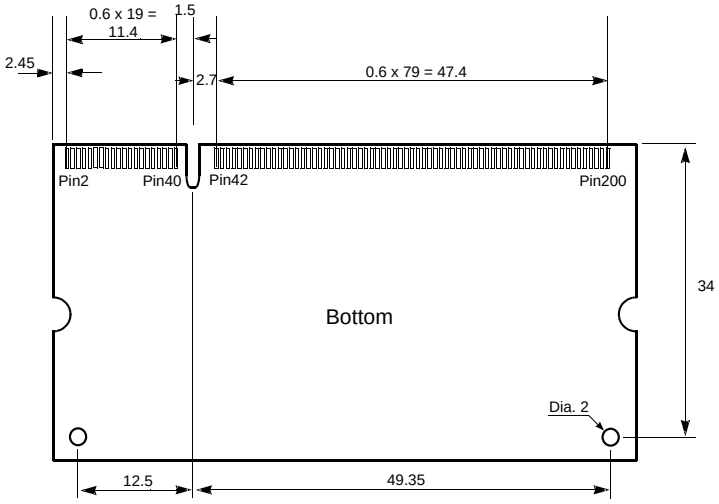


Figure 13: DH PXA270 Module Dimensions

6.3 Mechanical

Examples for mechanical counterparts are listed in this chapter.

6.3.1 SODIMM-200 Sockets

The DH PXA270 core module is designed for a regular 2.5V (DDR1) SODIMM-200 memory socket. The following sockets have been tested with the core module:

Tyco Electronics SODIMM Socket

http://www.tycoelectronics.com

Description: Socket height 5.2mm / underside space 1.0mm

→ Part number 1473005-1

Description: Socket height 9.2mm / underside space 5.0mm

→ Part number 1612618-1

NEXUS COMPONENTS

www.nexus-de.com

Description: Socket height 5.2mm / underside space 1.0mm

→ Part number 5214HB52

Description: Socket height 9.2mm / underside space 5.0mm

→ Part number 5214HB92

Foxconn Electronics Inc.

http://www.foxconn.com

Description: Socket height 5.2mm / underside space 1.0mm

→ Part number AS0A426-E2SN-7F

Typical DDR SO-DIMM Socket specifications:

- Durability: 25 cycles
- Voltage rating: 25V
- Current rating: 0.5A
- Contact resistance: 50mΩ max.
- Insulation resistance: 100MΩ
- Operating temperature: -40°C to +85°C

6.3.2 JTAG FFC cable

The following FFC cables have been tested with the core module JTAG connector:

Würth Elektronik 0.50mm flat flexible cable type 1 WR-FPC

→ Part number 687 610 050 002

http://www.we-online.com

Molex 0.50mm flat flexible cable type A

→ Part number 982660097

http://www.molex.com

6.4 Temperature Range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operation temperature range	-40		85	°C

Table 25: Operation Temperature Range

7 RoHS conformance

This device has been manufactured RoHS compliant.

List of Abbreviations

AUDMUX	Audio Multiplexer
BSP	Board Support Package
CSI	CMOS Sensor Interface
CSPI	Configurable Serial Peripheral Interface
EMI	Electromagnetic interference
FFC	Flat Flex Cable
MBC	must be connected
PU	Pull-Up
PD	Pull-Down
SSI	Synchronous Serial Interface
USB OTG	USB On-The-Go