

## **User Manual**

# **User Manual**

# **DHCOM AM35xx Module**



**Product:**     **DHCOM AM35xx Module**   Created by KH

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## **User Manual**

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## Changes

Version	Date	Changes	State	Name	Notes
1.0	30.09.2011	First issue			
1.1	16.11.2011	<ul style="list-style-type: none"><li>• Main features adapted</li><li>• Block circuit diagram (Chapter 2) replaced</li></ul>		HH	
1.2	27.06.2012	<ul style="list-style-type: none"><li>• Several notes added at the start of Chapter 3</li><li>• Figure 3 (Vbat GoldCap example) updated</li><li>• Ethernet LED circuitry (see 3.3)</li><li>• USB PHY and hub manufacturer details added (see 1.4.4)</li><li>• USB description adapted to current hardware status (see 3.4)</li><li>• USB USB_DRVVBUS detail (GPIO_E) removed (see 3.4.1)</li><li>• INT_HIGHEST_PRIORITY “active low” detail added (see 3.15)</li><li>• Comments added in USB chapter. (see 3.4)</li><li>• All full function pins listed at UART 1 (see 3.5.1)</li><li>• Latch details address removed (see 3.10)</li></ul>	released	AG	

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Version	Date	Changes	State	Name	Notes
		<ul style="list-style-type: none"><li>• Details for GPIO_L – GPIO_O removed, since these are used for the full function UART (see 3.15)</li><li>• Operating conditions updated (see 5.1)</li><li>• Dimension drawing updated (see 5.2)</li><li>• Amendment: What happens when the pin is not used</li><li>• Amending the “active low” details of the Reset_In and Reset_Out line (see 3.1)</li><li>• Designation “Not connected” replaced by “Reserved”.</li><li>• Note “Connection possibility to DHC<small>OM</small> UART 1” moved from Chapter 3.0 to 3.5.1.</li><li>• Ethernet LED pin “not used” information added (see 3.3)</li><li>• Core module power consumption added (see 5.1)</li><li>• USB Host 2: Supported USB speeds adapted (see 3.4.3)</li><li>• On-board I<sup>2</sup>C addresses added (see 3.7)</li><li>• Module general diagram revised (see 2.)</li><li>• ETH_VIO_SWITCHED absolute maximum ratings supplemented (see 5.1)</li></ul>			

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Version	Date	Changes	State	Name	Notes
1.3	16.07.2012	<ul style="list-style-type: none"><li>English translation</li></ul>	released	AG	
1.4	17.09.2012	<ul style="list-style-type: none"><li>OTG device speeds (see 3.4.1)</li></ul>	released	AG	
1.5	15.11.2012	<ul style="list-style-type: none"><li>Updated dimensions figure (see 5.2)</li></ul>	released	AG	
1.6	26.05.2014	<ul style="list-style-type: none"><li>Add RoHS conformance information</li></ul>	released	AG	
1.7	31.10.2014	<ul style="list-style-type: none"><li>Add differences between AM3505 and AM3517</li></ul>	released	AG	
1.8	xx.xx.xxxx	<ul style="list-style-type: none"><li>Changed LC_EN description from "LCD display enable" to "LCD display data enable"(see 3.11)</li></ul>	internal		



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## **1 Introduction**

### **1.1 Hardware**

The DHCM-AM35-01D2 module is a computer module in the SODIMM-200 form factor on the basis of a Cortex-A8 processor from Texas Instruments. The CPU is clocked at 600 MHz and is equipped with up to 512 MByte DDR2-SDRAM and 2048 MByte NAND flash. Numerous interfaces are also available for communicating with the outside world, which are required in embedded systems.

The pin assignment of the SODIMM 200 socket is subject to the DHCOM standard, so that a replacement or an upgrade to other DHCOM modules is very easily possible.

### **1.2 Software**

At present, the DHCM-AM35-01D2 module is available with the Windows Embedded Compact 7 and Embedded Linux operating systems.

The operating system images have all the necessary drivers for the interfaces. Board Support Packages (BSPs) are also available, with which the customer has the opportunity to generate its own customer-specific operating system image.

### **1.3 Main characteristics**

- Cortex-A8 Texas Instruments AM3505/17 @ 600MHz  
Differences: AM3517 includes the PowerVR™ SGX graphics engine which supports OPENGL® ES 2.0.
- 0 - 2048 MByte NAND flash memory (8 bit bus width)
- 4 MB SPI flash
- 64 - 512 MByte DDR2-333
- On-board microSD card socket
- SD/MMC card interface, 4 bit SDIO
- LC display controller, 24 bit colors, 1400x1050 pixels
- On-board touch controller for 4-wire resistive touch screens

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- Ethernet controller 10/100 Mbit, IEEE802.3 conform
- USB 2.0 OTG high-speed
- 2 x USB 2.0 host high speed (full and low speed will also be supported)
- Full function UART
- Standard UART with hardware handshake support
- Standard UART
- CAN interface
- 2 x SPI interface
- 2 x I2C<sup>TM</sup> interface
- I<sup>2</sup>S Audio codec (1 x microphone, 1 x Line in, 1x Line out)
- Real-time clock (I2C<sup>TM</sup> connection)
- Camera interface (BT. 656 - 10 bit)
- 12 bit analog input
- 1 kbit EEPROM with integrated MAC address
- 16 bit address/databus interface on SODIMM-200 socket
- PWM channel
- 9 GPIOs
- JTAG debug connection via FFC plug connector
- Industrial temperature range (-40°C to +85°C)
- SODIMM-200 socket with DHCOM pin assignment

### **1.4 Further technical information**

For more precise technical information, we refer you to the websites of the chip manufacturers:

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### **1.4.1 Texas Instruments AM35xx processor**

Data sheets and technical documents can be found at <http://www.ti.com>

### **1.4.2 Ethernet PHY LAN8710Ai**

Data sheets and technical documents can be found at <http://www.smsc.com>

### **1.4.3 Real-time clock MCP79411T-I/MS**

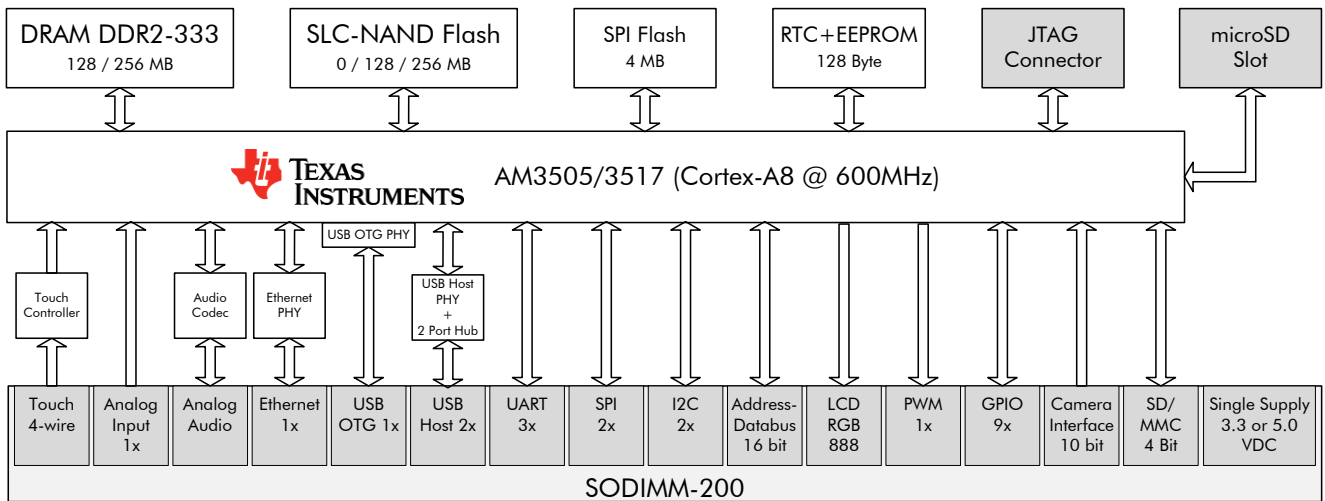
Data sheets and technical documents can be found at <http://www.microchip.com>

### **1.4.4 USB PHY USB3320 and USB Hub USB2512B**

Data sheets and technical documents can be found at <http://www.smsc.com>

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## 2 Hardware overview



**Figure 1: DHCM-AM35-01D2 block diagram**

Figure 1 provides an overview of the DHCM-AM35-01D2 module. All interfaces and memory components are shown.

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### **3 Signal description**

The following subsections describe the signals at the SODIMM-200 socket.

#### **Notes:**

- Where no basic function can be allocated to a pin (e.g. USB, I<sup>2</sup>C™, ...), then the GPIO designation is specified for the CPU pin.
- For all specified pull-up and pull-down resistors, a value of 10k is recommended.

#### **DHCOM hardware compatibility:**

The DHCOM specification specifies function groups in order to ensure compatibility between various DHCOM modules. Each function group has its own voltage level output (Vcam\_OUT, Vdisp\_OUT, Vsysbus\_OUT and VIO\_OUT). Level shifters on the customer specific main board provide compatibility between various DHCOM modules. Naturally, these level shifters can also be removed from the customer design. In this case, the customer will lose compatibility to the DHCOM standard.



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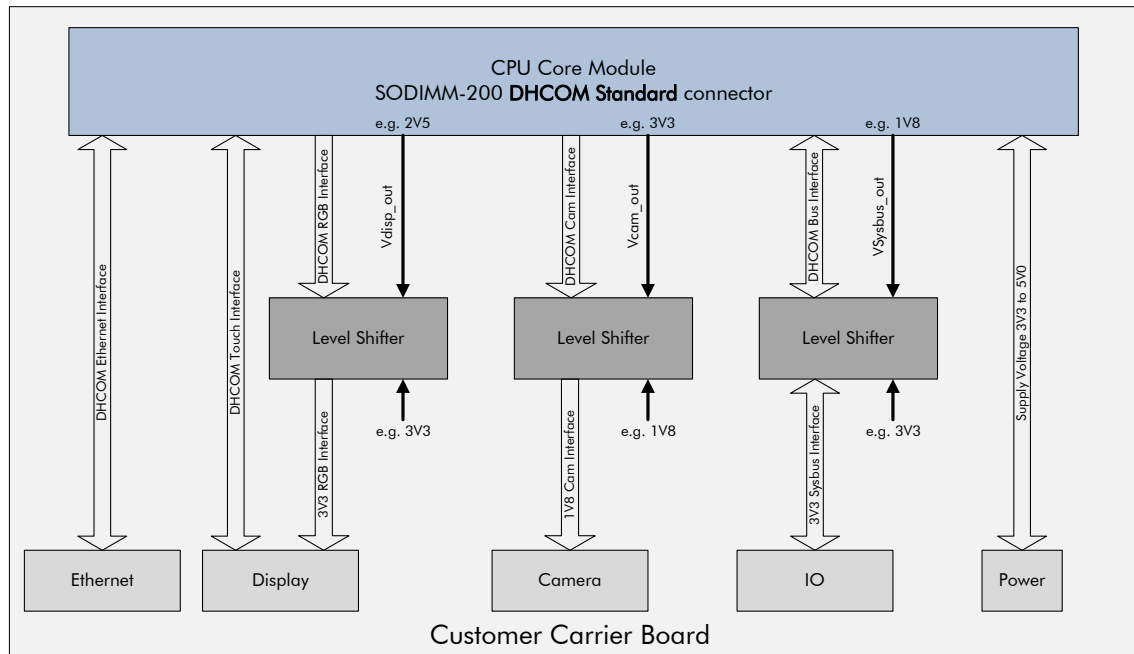


Figure 2: DHCOM functions groups concept

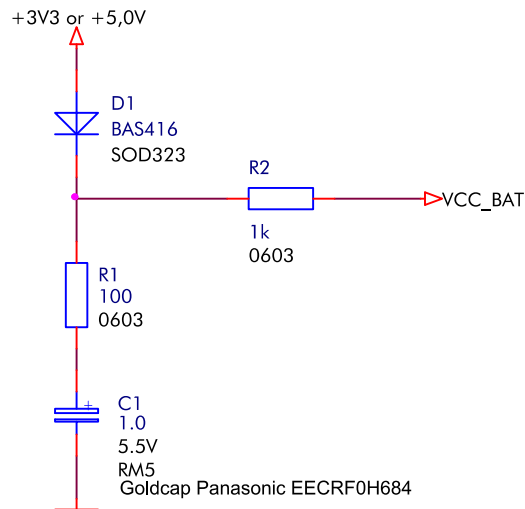
### 3.1 Power supply and reset

The DHCM-AM35-01D2 has the following power connections:

- $V_{in}$  = Core module supply voltage
- $V_{bat}$  = Battery voltage
- $V_{sysbus}$  = System bus voltage
- $V_{disp}$  = Display voltage
- $V_{cam}$  = Camera voltage
- $V_{IO}$  = I/O voltage

**Note:** When no buffer battery is used in the system,  $V_{bat}$  must be connected with 3.3V.

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**Figure 3: Vbat GoldCap example**

The power supply connections Vsysbus\_OUT, Vdisp\_OUT, Vcam\_OUT and VIO\_OUT are to be used to detect the right voltage level on the carrier board (1V8, 3V3, 5V0) and, where necessary, to adapt the voltage level with the level shifter.

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Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
VCC_IN1	Core Module supply voltage input	38	PWR_I	Dedicated Pin	MBC
VCC_IN2	Core Module supply voltage input	39	PWR_I	Dedicated Pin	MBC
VCC_IN3	Core Module supply voltage input	40	PWR_I	Dedicated Pin	MBC
VCC_IN4	Core Module supply voltage input	41	PWR_I	Dedicated Pin	MBC
VCC_IN5	Core Module supply voltage input	42	PWR_I	Dedicated Pin	MBC
VCC_IN6	Core Module supply voltage input	44	PWR_I	Dedicated Pin	MBC
GND1	Core Module Ground	17	PWR_I	Dedicated Pin	MBC
GND2	Core Module Ground	19	PWR_I	Dedicated Pin	MBC
GND3	Core Module Ground	43	PWR_I	Dedicated Pin	MBC
GND4	Core Module Ground	45	PWR_I	Dedicated Pin	MBC
GND5	Core Module Ground	47	PWR_I	Dedicated Pin	MBC
GND6	Core Module Ground	101	PWR_I	Dedicated Pin	MBC
GND7	Core Module Ground	111	PWR_I	Dedicated Pin	MBC
GND8	Core Module Ground	153	PWR_I	Dedicated Pin	MBC
GND9	Core Module Ground	185	PWR_I	Dedicated Pin	MBC
GND10	Core Module Ground	199	PWR_I	Dedicated Pin	MBC
VCC_BAT	Core Module Battery voltage input	200	PWR_I	Dedicated Pin	MBC
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	Dedicated Pin	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	Dedicated Pin	MBC

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Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	Dedicated Pin	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	Dedicated Pin	-
Vcam_OUT	Camera supply voltage output	102	PWR_O	Dedicated Pin	-
VIO_OUT	I/O supply voltage output	152	PWR_O	Dedicated Pin	-
RESET_IN	System Reset input (active low)	21	I	Dedicated Pin	-
RESET_OUT	System Reset output (active low)	20	O	Dedicated Pin	-

**Table 1: Power supply and reset**

## **3.2 Touch controller / Analog inputs**

The DHCM-AM35-01D2 module is equipped with a 4-Wire 12 bit resistive Touch Controller (Texas Instruments TSC2004), which is connected via I<sup>2</sup>C™ with the AM35xx processor. In addition, this touch controller offers an analog input for, e.g. temperature or voltage measurements, which is also administered on the SODIMM-200 connections.

- I<sup>2</sup>C™ Address Touch Controller TSC2004: 0x4B

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

<http://www.ti.com/>

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Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
TSPX	Resistive Touch: 4 wire (X +)	12	AINOUT	Dedicated Pin	PD
TSMX	Resistive Touch: 4 wire (X -)	14	AINOUT	Dedicated Pin	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	AINOUT	Dedicated Pin	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	AINOUT	Dedicated Pin	PD

**Table 2: Touch controller connections**

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
Analog_In0	Analog input 0	8	AIN	Dedicated Pin	PD

**Table 3: Analog inputs**

### 3.3 Ethernet

The AM35xx processor includes a 10/100 Ethernet Media Access Controller (MAC). A 10/100 Ethernet transceiver (SMSC LAN8710Ai) is connected on the module at this interface. This Ethernet interface fulfils the IEEE 802.3-2005 standard.

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments and SMSC.

<http://www.ti.com/>

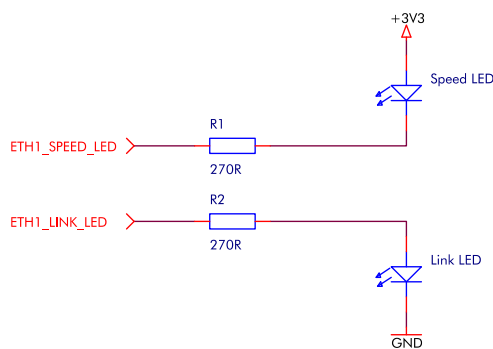
<http://www.smSC.com/>

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Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	Dedicated Pin	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	Dedicated Pin	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	Dedicated Pin	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	Dedicated Pin	PD
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	Dedicated Pin	-
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	Dedicated Pin	PD
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	Dedicated Pin	PD

**Table 4: Ethernet connections**

**Note:** The LED outputs “nETH1\_LINK\_LED” and “nETH1\_SPEED\_LED” must be connected as follows:



**Figure 4: Ethernet LED circuitry**

**Note:** In addition to their LED function, the Ethernet PHY LEDs are also used as reset configuration lines.

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### 3.4 USB

The DHCOM-AM35xx-01D2 module supports a maximum of three USB devices. These consist of a USB OTG connection and two USB host connections. For the USB OTG, the integrated AM35xx PHY is used. For the USB host connections, a USB transceiver (SMSC USB3320) is connected via the ULPI interface to the AM35xx. Downstream of the USB transceiver, there is an additional USB hub (SMSC USB2512B) to generate the second host port.

All three ports are high-speed USB connections, which also support full speed and low speed.

#### 3.4.1 USB OTG (AM35xx integrated PHY)

This USB interface fulfils the USB 2.0 specification. It can be configured as OTG, host or device. As a host, it supports peripheral devices of all speeds and as a peripheral, it communicates at either high-speed (480Mbps) or full speed (12Mbps) when connected to legacy host computers.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
USB_OTG_VBUS	OTG Client: VBUS Input line  OTG Host: USB bus supply voltage	166	I /  PWR_O	Dedicated Pin	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	Dedicated Pin	-
USB_OTG_D+	USB OTG differential Signal positive line	170	IO	Dedicated Pin	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	IO	Dedicated Pin	PD

**Table 5: USB OTG**

**Note:** The DHCOM USB OTG port does not provide any “enable” and “over current” signals. The ID connection from the USB cable should be used for switching the VBUS on and off. To detect an over current event, the “over current” output of the USB power management IC can be connected to one of the DHCOM GPIOs. This GPIO can then be independently monitored by the customer.

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### 3.4.2 USB Host 1

The USB Host 1 port fulfils the USB 2.0 specification. It supports high-speed, full speed and low speed data transfers.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
USB_PWR_STAT	USB Host over current indicator (active low)	174	I	Dedicated Pin	-
USB_PWR_EN	USB Host power enable signal (active low)	176	O	Dedicated Pin	-
USB_HOST_D1+	USB Host differential Signal positive line	178	IO	Dedicated Pin	PD
USB_HOST_D1-	USB Host differential Signal negative line	180	IO	Dedicated Pin	PD

**Table 6: USB Host 1**

### 3.4.3 USB Host 2

The USB Host 2 port fulfils the USB 2.0 specification. It supports high-speed, full speed and low speed data transfers.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
USB_HOST_D2+	USB Host differential Signal positive line	169	IO	Dedicated Pin	PD
USB_HOST_D2-	USB Host differential Signal negative line	171	IO	Dedicated Pin	PD

**Table 7: USB Host 2**

**Note:** The “USB\_PWR\_STAT” and “USB\_PWR\_EN” signals are used for Host 1 as well as for Host 2, i.e. the bus voltage is always switched on or off simultaneously for both ports.



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### 3.5 UART

The DHCM-AM35-01D2 module offers connections for a total of three UARTs. These UARTs are based on the 16C750 model. UART 1 and UART 2 additionally support a hardware handshake.

The maximum transfer rate is 5 Mbit/s.

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

<http://www.ti.com/>

#### 3.5.1 UART 1

**Note:** DHCOM UART 1 is the UART 1 module of the AM35xx.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
UART1_DTR	Full function UART data terminal ready	22	O	GPIO_136	-
UART1_CTS	UART clear to send	24	I	GPIO_150	-
UART1_RTS	UART request to send	26	O	GPIO_149	-
UART1_DSR	Full function UART data set ready	28	I	GPIO_137	-
UART1_DCD	Full function UART data carrier detect	30	I	GPIO_138	-
UART1_RX	UART receive data line	32	I	GPIO_151	-
UART1_TX	UART transmit data line	34	O	GPIO_148	-
UART1_RI	Full function UART ring indicator	36	I	GPIO_139	-

Table 8: UART 1

**Hardware design notes:**

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- It is essential to always create a possible connection to DHCOM UART 1, since the DHCOM bootloader can be operated with the UART 1. A minimum connection possibility should be made available via solder pads.

### 3.5.2 UART 2

**Note:** DHCOM UART 2 is the UART 3 module of the AM35xx.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
UART2_CTS	UART clear to send	31	I	GPIO_163	-
UART2_RTS	UART request to send	33	O	GPIO_164	-
UART2_RX	UART receive data line	35	I	GPIO_165	-
UART2_TX	UART transmit data line	37	O	GPIO_166	-

Table 9: UART 2

### 3.5.3 UART 3

**Note:** DHCOM UART 3 is the UART 2 module of the AM35xx.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
UART3_RX	Serial port receive data line	23	I	GPIO_143	-
UART3_TX	Serial port transmit data line	25	O	GPIO_142	-

Table 10: UART 3

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### **3.6 Serial port interface**

The DHCM-AM35-01D2 module is equipped with two SPI interfaces. These interfaces consist of a full duplex capable, 4-wire interface and have the following characteristics:

- Master/slave functionality
- Full-duplex / Half-duplex
- Serial clock with programmable frequency, polarity and phase
- Word length from 4 bit to 32 bit
- 64 bytes built-in FIFO
- Maximum clock frequency up to 48MHz

For more precise information, we refer here to the data sheet and other technical documents of Texas Instruments.

<http://www.ti.com/>

#### **Notes:**

- DHCOM SPI Port 1 is connected to the MCSPI1 interface of the AM35xx
- SPI1\_CS0 on the SODIMM-200 socket uses the MCSPI1\_CS1 signal of the AM35xx
- The MCSPI1 interface of the AM35xx is also used for the on-board SPI flash
- MCSPI1\_CS0 is used for the on-board SPI flash

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Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
SPI1_CS0	Slave select signal	177	O	GPIO_175	-
SPI1_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	GPIO_171	-
SPI1_MISO	SSP receive data line	181	I	GPIO_173	-
SPI1_MOSI	SSP transmit data line	183	O	GPIO_172	-

**Table 11: SPI1 Interface**

### Notes:

- DHCAM SPI Port 2 is connected to the MCSPI2 interface of the AM35xx

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
SPI2_CS0	Slave select signal	155	O	GPIO_181	-
SPI2_CLK	SPI clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	157	IO	GPIO_178	-
SPI2_MISO	SSP receive data line	159	I	GPIO_180	-
SPI2_MOSI	SSP transmit data line	161	O	GPIO_179	-

**Table 12: SPI2 Interface**

## 3.7 I<sup>2</sup>C

The DHCAM-AM35-01D2 module provides the opportunity to connect up to two separate I<sup>2</sup>C™ multimaster buses. The I<sup>2</sup>C™ bus controller integrated in the AM35xx has the following main features:

- Fulfills Philips I<sup>2</sup>C™ specification 2.1

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- Standard mode (100 kbit/s) and fast mode (400 kbit/s)
- 7 bit and 10 bit device addressing
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode

The pull-up resistors required according to the I<sup>2</sup>C™ specification are already fitted on the module.

For detailed information about I<sup>2</sup>C™, reference is made to the specification (Philips Semiconductor):

<http://www.nxp.com>

**Note:** DHCOM I2C1 uses the I2C3 instance of the AM35xx.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
I2C1_CLK	I <sup>2</sup> C clock line	182	IO	GPIO_184	-
I2C1_DATA	I <sup>2</sup> C data line	184	IO	GPIO_185	-

**Table 13: I2CTM Port 1**

**Note:** DHCOM I2C2 uses the I2C2 instance of the AM35xx.

## **User Manual**

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
I2C2_CLK	I <sup>2</sup> C clock line	158	IO	GPIO_168	-
I2C2_DATA	I <sup>2</sup> C data line	160	IO	GPIO_183	-

**Table 14: I2C™ Port 2**

**Note:** The I2C1 instance of the AM35xx is used on the core module for the following modules:

- RTC EEPROM (7 bit address: 0x57)
- RTC (7 bit address: 0x6F)
- Audio codec (7 bit address: 0x1A)
- PMIC (7 bit address: 0x48)
- Touch controller (7 bit address: 0x4B)

### **3.8 CAN**

The AM35xx processor has an integrated standard resp. high-end CAN controller.

Main characteristics:

- Standard CAN controller (SCC) for standard CAN applications
- High-end CAN controller (HECC) for complex applications
- Fully compliant with CAN protocol, version 2.0B
- Standard / extended identifiers
- Speed up to 1 Mbps
- Programmable bit time and sampling mode (1x or 3x)
- Selectable edge of receive bit flow for synchronization

## **User Manual**

- Bus failure diagnostic

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
CAN_TX	CAN transmit data line	27	IO	GPIO_130	-
CAN_RX	CAN receive data line	29	IO	GPIO_131	-

**Table 15: CAN interface**

### **3.9 Audio interface**

The DHCM-AM35-01D2 module is equipped with an Audio Codec module (Texas Instruments TLV320AIC23B), through which the line connection is made with a microphone, headphone or device.

## User Manual

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	Dedicated Pin	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	Dedicated Pin	MBC
MIC_IN	Microphone Input Signal	1	I	Dedicated Pin	PD
MIC_GND	Microphone Ground	3	PWR_I	Dedicated Pin	-
LINEIN_L	Line-In Left	5	I	Dedicated Pin	PD
LINEIN_R	Line-In Right	7	I	Dedicated Pin	PD
HP_GND	Headphone Ground	11	PWR	Dedicated Pin	-
HP_OUT_LEFT	Headphone Output left	13	O	Dedicated Pin	-
HP_OUT_RIGHT	Headphone Output right	15	O	Dedicated Pin	-

**Table 16: Audio interface**

**Note:** If the audio inputs are not used, they must be closed with a pull-down. The resistor must be connected with VSSA\_Audio.

### 3.10 Address and data bus

The DHCM-AM35-01D2 module supports the connection of peripheral devices via a parallel address and data bus, by using the AM35xx memory bus interface (General Purpose Memory Controller GPMC).

A more precise description for this interface is available in the reference manual of the AM35xx <http://www.ti.com/>

**Note:**

- GPMC\_nCS0 is used for the on-board NAND flash.



# User Manual

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	Dedicated Pin	-
A00 – A15	Memory controller address line	See Chapter 4	O	Dedicated Pins	-
D00 – D15	Memory controller data line	See Chapter 4	IO	Dedicated Pins	-
CS_A	Static memory chip select 0	128	O	GPMC_nCS1 GPIO_52	-
CS_B	Static memory chip select 1	129	O	GPMC_nCS2 GPIO_53	-
CS_C	Static memory chip select 3	130	O	GPMC_nCS3	-
CS_D	Static memory chip select 4	131	O	GPMC_nCS4	-
CS_E	Static memory chip select 5	132	O	GPMC_nCS5	-
WE	Memory controller write enable	133	O	GPMC_nWE	-
OE	Memory controller output enable	134	O	GPMC_nOE	-

**Table 17: Address and data bus**

## 3.11 LCD controller

The DHCOM-AM35-01D2 module enables the connection of a 24 bit LCD display. Active as well as passive LCD displays with a resolution of up to 1400 x 1050 pixels can be operated. A parallel RGB888 interface can be used for connection to the display.

The core of the LCD controller is the integrated display subsystem in the AM35xx. More precise information about this is available in the AM35xx Reference Manual:

<http://www.ti.com/>

## **User Manual**

### **3.11.1 RGB888 Display Interface**

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	Dedicated Pin	-
LC_R0	LCD display data red 0	76	O	GPIO_86	-
LC_R1	LCD display data red 1	78	O	GPIO_87	-
LC_R2	LCD display data red 2	49	O	GPIO_88	-
LC_R3	LCD display data red 3	51	O	GPIO_89	-
LC_R4	LCD display data red 4	53	O	GPIO_90	-
LC_R5	LCD display data red 5	55	O	GPIO_91	-
LC_R6	LCD display data red 6	57	O	GPIO_92	-
LC_R7	LCD display data red 7	59	O	GPIO_93	-
LC_G0	LCD display data green 0	80	O	GPIO_78	-
LC_G1	LCD display data green 1	82	O	GPIO_79	-
LC_G2	LCD display data green 2	61	O	GPIO_80	-
LC_G3	LCD display data green 3	63	O	GPIO_81	-
LC_G4	LCD display data green 4	65	O	GPIO_82	-
LC_G5	LCD display data green 5	67	O	GPIO_83	-
LC_G6	LCD display data green 6	69	O	GPIO_84	-
LC_G7	LCD display data green 7	71	O	GPIO_85	-
LC_B0	LCD display data blue 0	84	O	GPIO_70	-
LC_B1	LCD display data blue 1	86	O	GPIO_71	-

## User Manual

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
LC_B2	LCD display data blue 2	73	O	GPIO_72	-
LC_B3	LCD display data blue 3	75	O	GPIO_73	-
LC_B4	LCD display data blue 4	77	O	GPIO_74	-
LC_B5	LCD display data blue 5	79	O	GPIO_75	-
LC_B6	LCD display data blue 6	81	O	GPIO_76	-
LC_B7	LCD display data blue 7	83	O	GPIO_77	-
LC_EN	LCD display data enable	85	O	GPIO_69	-
LC_VSYNC	LCD frame or vertical sync. puls	87	O	GPIO_68	-
LC_HSYNC	LCD line or horizontal sync. puls	89	O	GPIO_67	-
LC_PCLK	LCD pixel clock	91	O	GPIO_66	-
GPIO_PWM	LCD contrast (only if PWM is not used)	100	O	GPIO_57	-

**Table 18: Display interface RGB888**

### 3.11.2 LVDS display interface

The DHCAM-AM35-01D2 module is not currently available as a LVDS interface for connection of a display.

If necessary, the Texas Instruments flat link transmitter (SN75LVDS83B) can be used on the carrier board to generate the required signals.

<http://www.ti.com/product/sn75lvds83b>

### 3.12 PWM

The signal at pin 100 of the DHCAM-AM35-01D2 module can be used as a PWM signal.

## User Manual

**Note:** GPIO\_PWM is mapped on the GPT11\_PWM\_EVT signal of the AM35xx.

For further information, reference is made here to Chapter 13 “Timers” in the AM35xx Reference Manual:

<http://www.ti.com/>

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
GPIO_PWM	PWM channel (only if LCD contrast is not used)	100	O	GPIO_57	-

**Table 19: PWM**

### 3.13 SD/MMC/SDIO controller

The AM35xx processor has a SD/MMC/SDIO card host controller integrated. Two controllers are used on the module, one for access to the on-board microSD card, the other as a SD/MMC/SDIO interface to the SODIMM-200 socket.

Main characteristics:

- Multimedia Card System Specification 4.2
- SD Memory Card Specifications 2.0
- SDIO Card Specification, Part E1, v1.10
- 1 bit or 4 bit transfer mode
- 1024 byte buffer for read or write

#### 3.13.1 On-board microSD card socket

This interface uses the SD/MMC/SDIO Controller 1 of the AM35xx.

## User Manual

Signal Name	Description	µSD Socket Pin Number	IO Type	Multiplexed
SD_CLK	SD/SDIO/MMC bus clock	5	O	GPIO_120
SD_CMD	SD/SDIO/MMC command line	3	IO	GPIO_121
SD_DETECT	SD/SDIO/MMC card detection (LOW when card inserted)	G3	I	GPIO_127
SD_D0	SD/SDIO/MMC data line	7	IO	GPIO_122
SD_D1	SD/SDIO/MMC data line	8	IO	GPIO_123
SD_D2	SD/SDIO/MMC data line	1	IO	GPIO_124
SD_D3	SD/SDIO/MMC data line	2	IO	GPIO_125

**Table 20: On-board microSD card socket**

### 3.13.2 SD/MMC/SDIO interface

This interface uses the SD/MMC/SDIO Controller 2 of the AM35xx.

## User Manual

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	GPIO_130	-
SD_CMD	SD/SDIO/MMC command line	104	IO	GPIO_131	-
SD_DETECT	SD/SDIO/MMC card detection(active high)	105	I	GPIO_126	PD
SD_D0	SD/SDIO/MMC data line	106	IO	GPIO_132	-
SD_D1	SD/SDIO/MMC data line	107	IO	GPIO_133	-
SD_D2	SD/SDIO/MMC data line	108	IO	GPIO_134	-
SD_D3	SD/SDIO/MMC data line	109	IO	GPIO_135	-

**Table 21: MMC/SD/SDIO card interface**

### 3.14 Camera/image sensor interface

The DHCAM-AM35-01D2 module permits connection of an external camera or an image sensor. This makes use of the Video Processing Front End (VPFE) integrated in the AM35xx. This has the following main features:

- Supports conventional Bayer pattern sensors and Foveon sensors
- Flexible synchronization timing generation
- Supports progressive and interlaced sensors
- Max. pixel clock 75 MHz
- Supports REC656, CCIR-656, YCbCr422 standard

Note: The DHCAM standard only supports a data width of 10 bit on the SODIMM-200 socket.

For further information, reference is made here to Chapter 10 “VPFE Controller” in the AM35xx Reference Manual: <http://www.ti.com/>

# User Manual

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
Vcam_OUT	Camera supply voltage output	102	PWR_O	Dedicated Pin	-
CIF_D0	CSI Interface Data line 0	48	I	GPIO_99	-
CIF_D1	CSI Interface Data line 1	50	I	GPIO_100	-
CIF_D2	CSI Interface Data line 2	52	I	GPIO_101	-
CIF_D3	CSI Interface Data line 3	54	I	GPIO_102	-
CIF_D4	CSI Interface Data line 4	56	I	GPIO_103	-
CIF_D5	CSI Interface Data line 5	58	I	GPIO_104	-
CIF_D6	CSI Interface Data line 6	60	I	GPIO_105	-
CIF_D7	CSI Interface Data line 7	62	I	GPIO_106	-
CIF_D8	CSI Interface Data line 8	64	I	GPIO_95	-
CIF_D9	CSI Interface Data line 9	66	I	GPIO_98	-
CIF_VSYNC	CSI Interface Frame Synchronization	68	I	GPIO_97	-
CIF_MCLK	CSI Interface Master Clock output	70	O	GPT8_PWM_EV T GPIO_58	-
CIF_PCLK	CSI Interface Pixel Clock input	72	I	GPIO_94	-
CIF_HSYNC	CSI Interface Line Synchronization	74	I	GPIO_96	-

Table 22: Camera/image sensor interface

## 3.15 GPIOs

The DHCAM-AM35-01D2 module provides several GPIO pins on the SODIMM-200 socket. These are freely available for any functions (see Table 23).

## User Manual

Many of the other pins with alternative functions can also be configured as GPIO, if the originally allocated function isn't needed. In this case, the customer will lose compatibility to the DHC0M standard.

Pin Name	Description	SODIMM Pin Number	IO Type	Multiplexed	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	IO	GPIO_0	PU
GPIO_A	General Purpose I/O	154	IO	GPIO_116	-
GPIO_B	General Purpose I/O	156	IO	GPIO_117	-
GPIO_C	General Purpose I/O	162	IO	GPIO_118	-
GPIO_D	General Purpose I/O	163	IO	GPIO_119	-
GPIO_E	General Purpose I/O	164	IO	GPIO_125	-
GPIO_F	General Purpose I/O	165	IO	GPIO_140	-
GPIO_G	General Purpose I/O	167	IO	GPIO_141	-
GPIO_H	General Purpose I/O	173	IO	GPIO_155	-
GPIO_I	General Purpose I/O	175	IO	GPIO_152	-
VIO_OUT	Voltage for external Level-Shifter	152	PWR_O	Dedicated Pin	-

**Table 23: GPIO pin assignment**

Note: The GPIOs of the AM35xx can only drive at a maximum of 2mA. Where a greater current is required, an additional driver must be provided on the carrier board. The minimum and maximum logic level can be obtained from the data sheet of the AM35xx.

<http://www.ti.com/>



## User Manual

In the DHCOM product line there are additional modules (e.g. i.MX), which are compatible with the DHCOM standard (SODIMM-200 pin assignment). To ensure a possible exchange or upgrade/downgrade to some other module, several aspects need to be taken into account.

On the DHCM-iMX25-01D2 module, additional level shifters (Texas Instruments TXS0108E) are used for the GPIO signals, which raise the GPIO signal to a voltage level of 3.3V (Figure 5). Due to their design (automatic direction detection), these can only drive a current of  $< 100\mu\text{A}$  (strongly load dependent). For this reason, it is recommended that GPIO signals, which are operated as outputs, be provided on the carrier board with an additional driver circuit (e.g. SN74AHC1G125) or a transistor stage (Figure 6).

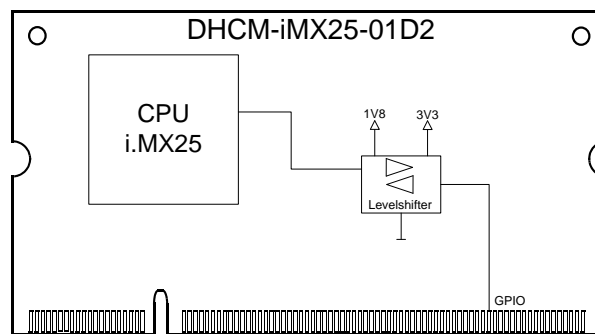


Figure 5: GPIO circuitry on DHCM-iMX25-01D2

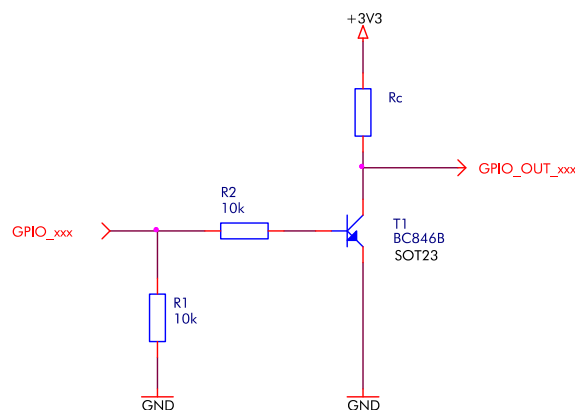


Figure 6: GPIO circuitry as output

**Product:**     **DHCOM AM35xx Module**   Created by KH

Date of creation: 30. September 2011

DHCOM AM35xx Module - User Manual eng



## **User Manual**

 [www.dh-electronics.de](http://www.dh-electronics.de)

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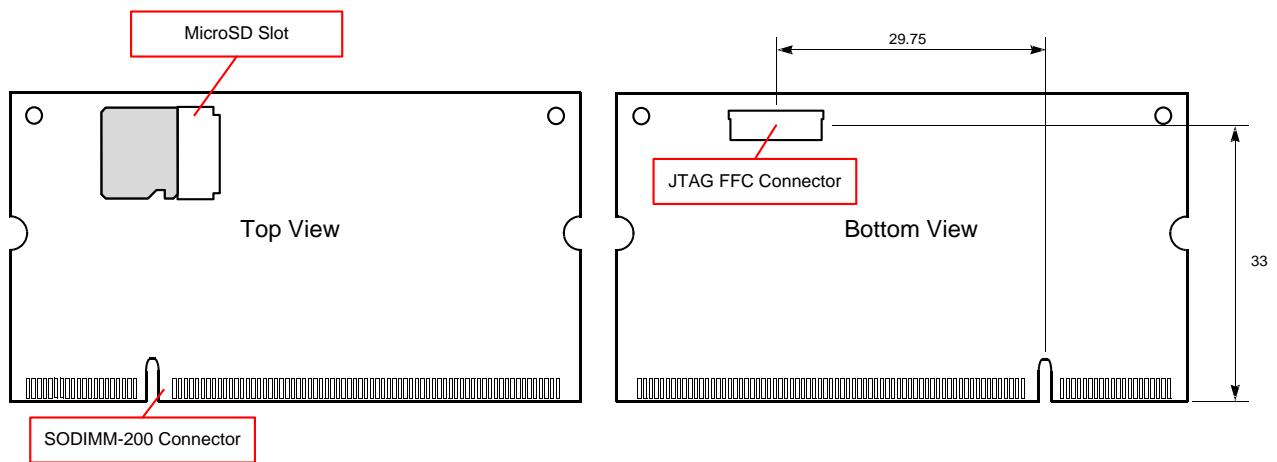
Voltage VIO\_OUT is output at pin 152 of the SODIMM-200 socket. This should be used to detect the voltage level on a carrier board.

Reason: If the DHCOM product line is extended in future with new modules, which can only output 1.8 V at the GPIO pins, compatibility would no longer apply. To avoid this, we recommend that the signal level be adapted with a level shifter on the carrier board.

## User Manual

### 4 Plugs and connections

Additionally to the SODIMM-200 connector, the DHCM-AM35-01D2 module is equipped with a 10pin FFC JTAG connector and a separate microSD card socket.



**Figure 7: Position of the plugs and connections**

## User Manual

### 4.1 SODIMM-200

Pin Number	Pin Name	Power Domain
1	Microphone In	VDDA
3	Microphone GND	VDDA
5	Line-In Left	VDDA
7	Line-In Right	VDDA
9	VSSA (Audio Supply GND)	VDDA
11	Headphone GND	VIO
13	Headphone Left	VDDA
15	Headphone Right	VDDA
17	GND1	Vin
19	GND2	Vin
21	RESET_IN	VIO
23	UART3_RX	VIO
25	UART3_TX	VIO
27	CAN_TX	VIO
29	CAN_RX	VIO
31	UART2_CTS	VIO
33	UART2_RTS	VIO
35	UART2_RX	VIO
37	UART2_TX	VIO

Pin Number	Pin Name	Power Domain
2	<i>Reserved</i>	
4	<i>Reserved</i>	
6	<i>Reserved</i>	
8	Analog Input 0	VDDA
10	VDDA (Audio Supply VCC)	VDDA
12	TSPX	VDDA
14	TSMX	VDDA
16	TSMY	VDDA
18	TSPY	VDDA
20	RESET_OUT	VIO
22	UART1_DTR	VIO
24	UART1_CTS	VIO
26	UART1_RTS	VIO
28	UART1_DSR	VIO
30	UART1_DCD	VIO
32	UART1_RX	VIO
34	UART1_TX	VIO
36	UART1_RI	VIO
38	VCC_IN1	Vin

## User Manual

Pin Number	Pin Name	Power Domain
39	VCC_IN2	Vin
41	VCC_IN4	Vin
43	GND3	Vin
45	GND4	Vin
47	GND5	Vin
49	LC_R2	Vdisp
51	LC_R3	Vdisp
53	LC_R4	Vdisp
55	LC_R5	Vdisp
57	LC_R6	Vdisp
59	LC_R7	Vdisp
61	LC_G2	Vdisp
63	LC_G3	Vdisp
65	LC_G4	Vdisp
67	LC_G5	Vdisp
69	LC_G6	Vdisp
71	LC_G7	Vdisp
73	LC_B2	Vdisp
75	LC_B3	Vdisp

Pin Number	Pin Name	Power Domain
40	VCC_IN3	Vin
42	VCC_IN5	Vin
44	VCC_IN6	Vin
46	Vdisp_OUT	Vdisp
48	CIF_D0	Vcam
50	CIF_D1	Vcam
52	CIF_D2	Vcam
54	CIF_D3	Vcam
56	CIF_D4	Vcam
58	CIF_D5	Vcam
60	CIF_D6	Vcam
62	CIF_D7	Vcam
64	CIF_D8	Vcam
66	CIF_D9	Vcam
68	CIF_VSYNC	Vcam
70	CIF_MCLK	Vcam
72	CIF_PCLK	Vcam
74	CIF_HSYNC	Vcam
76	LC_R0	Vdisp

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Pin Number	Pin Name	Power Domain
77	LC_B4	Vdisp
79	LC_B5	Vdisp
81	LC_B6	Vdisp
83	LC_B7	Vdisp
85	LC_EN	Vdisp
87	LC_VSYNC	Vdisp
89	LC_HSYNC	Vdisp
91	LC_PCLK	Vdisp
93	LVDS_TX2+	Vdisp
95	LVDS_TX2-	Vdisp
97	LVDS_CLK+	Vdisp
99	LVDS_CLK-	Vdisp
101	GND6	Vin
103	SD_CLK	VIO
105	SD_DETECT	VIO
107	SD_D1	VIO
109	SD_D3	VIO
111	GND7	Vin
113	<i>Reserved</i>	

Pin Number	Pin Name	Power Domain
78	LC_R1	Vdisp
80	LC_G0	Vdisp
82	LC_G1	Vdisp
84	LC_B0	Vdisp
86	LC_B1	Vdisp
88	LVDS_TX0+	Vdisp
90	LVDS_TX0-	Vdisp
92	LVDS_TX1+	Vdisp
94	LVDS_TX1-	Vdisp
96	<i>Reserved</i>	
98	<i>Reserved</i>	
100	GPIO_PWM	VIO
102	Vcam_OUT	Vcam
104	SD_CMD	VIO
106	SD_D0	VIO
108	SD_D2	VIO
110	Vsysbus_OUT	Vsysbus
112	A8	Vsysbus
114	A9	Vsysbus

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Pin Number	Pin Name	Power Domain
115	A1	Vsysbus
117	A2	Vsysbus
119	A3	Vsysbus
121	A4	Vsysbus
123	A5	Vsysbus
125	A6	Vsysbus
127	A7	Vsysbus
129	CS_B	Vsysbus
131	CS_D	Vsysbus
133	WE	Vsysbus
135	D0	Vsysbus
137	D1	Vsysbus
139	D2	Vsysbus
141	D3	Vsysbus
143	D4	Vsysbus
145	D5	Vsysbus
147	D6	Vsysbus
149	D7	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO

Pin Number	Pin Name	Power Domain
116	A10	Vsysbus
118	A11	Vsysbus
120	A12	Vsysbus
122	A13	Vsysbus
124	A14	Vsysbus
126	A15	Vsysbus
128	CS_A	Vsysbus
130	CS_C	Vsysbus
132	CS_E	Vsysbus
134	OE	Vsysbus
136	D8	Vsysbus
138	D9	Vsysbus
140	D10	Vsysbus
142	D11	Vsysbus
144	D12	Vsysbus
146	D13	Vsysbus
148	D14	Vsysbus
150	D15	Vsysbus
152	VIO_OUT	VIO

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Pin Number	Pin Name	Power Domain
153	GND8	Vin
155	SPI2_CS0	VIO
157	SPI2_CLK	VIO
159	SPI2_MISO	VIO
161	SPI2_MOSI	VIO
163	GPIO_D	VIO
165	GPIO_F	VIO
167	GPIO_G	VIO
169	USB_HOST_D2+	VIO
171	USB_HOST_D2-	VIO
173	GPIO_H	VIO
175	GPIO_I	VIO
177	SPI1_CS0	VIO
179	SPI1_CLK	VIO
181	SPI1_MISO	VIO
183	SPI1_MOSI	VIO
185	GND9	Vin
187	<i>Reserved</i>	
189	<i>Reserved</i>	

Pin Number	Pin Name	Power Domain
154	GPIO_A	VIO
156	GPIO_B	VIO
158	I2C2_CLK	VIO
160	I2C2_DATA	VIO
162	GPIO_C	VIO
164	USB_DRVVBUS (GPIO_E)	VIO
166	USB_OTG_VBUS	VIO
168	USB_OTG_ID	VIO
170	USB_OTG_D+	VIO
172	USB_OTG_D-	VIO
174	USB_PWR_STAT	VIO
176	USB_PWR_EN	VIO
178	USB_HOST_D1+	VIO
180	USB_HOST_D1-	VIO
182	I2C1_CLK	VIO
184	I2C1_DATA	VIO
186	nETH1_LINK_LED	VIO
188	nETH1_SPEED_LED	VIO
190	ETH1_TXD-	VIO



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Pin Number	Pin Name	Power Domain	Pin Number	Pin Name	Power Domain
191	<i>Reserved</i>		192	ETH1_TXD+	VIO
193	<i>Reserved</i>		194	ETH_VIO_SWITCHED	VIO
195	<i>Reserved</i>		196	ETH1_RXI-	VIO
197	<i>Reserved</i>		198	ETH1_RXI+	VIO
199	GND10	Vin	200	VCC_BAT	Vbat

Table 24: SODIMM-200 pin assignment

### 4.2 JTAG

Pin Number	Pin Name
1	+3V3 Output
2	GND
3	JTAG_TMS
4	#JTAG_TRST
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	JTAG_RTCK
10	i.MX25 DE_B pad

Table 25: JTAG interface pin assignment

# User Manual

## 5 Technical specifications

### 5.1 Operating conditions – Absolute maximum ratings

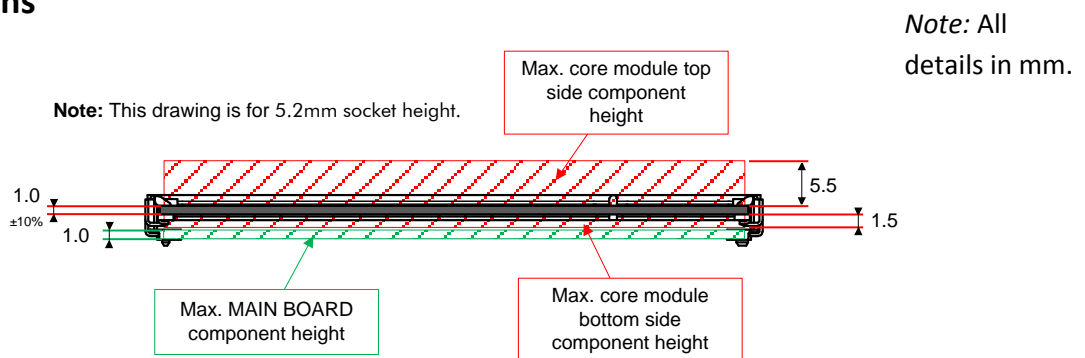
Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT	2.5		6.0	V
V <sub>bat</sub>	Battery voltage INPUT	1.3V		5.5	V
V <sub>sysbus</sub>	System bus voltage OUTPUT		3.3		V
I <sub>Vsysbus</sub>	Vsysbus current			20	mA
V <sub>disp</sub>	Display voltage OUTPUT		3.3		V
I <sub>Vdisp</sub>	Vdisp current			20	mA
V <sub>cam</sub>	Camera voltage OUTPUT		3.3		V
I <sub>Vcam</sub>	Vcam current			20	mA
V <sub>IO</sub>	I/O voltage OUTPUT		3.3		V
I <sub>VIO</sub>	VIO current			20	mA
V <sub>ETH_VIO_SWITCHED</sub>	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
I <sub>ETH_VIO_SWITCHED</sub>	ETH_VIO_SWITCHED current			60	mA
I	Operating current (without V*_OUT pins, VCC = 3.3V)		420	600	mA
Power (Vin)	AM35xx core module power consumption		1400	2000	mW
I <sub>Vbat</sub>	Vbat input current			5	mA
I <sub>Vbat_Stby</sub>	Vbat Standby input current			700	nA
V <sub>IH_3V3</sub>	Digital input high voltage	2.0	3.3		V

# User Manual

Symbol	Description	Min	Typ	Max	Unit
V <sub>IL_3V3</sub>	Digital input low voltage		0	0.8	V

**Table 26: DC operating conditions**

## 5.2 Dimensions



**Figure 8: Maximum heights**



## **User Manual**

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### **5.3 Mechanical system**

Several suggestions are given for the plugs, sockets and cables in the following subsections.

#### **5.3.1 SODIMM-200 socket**

The DHCM-AM35-01D2 module is designed for operation in a standard 2.5V (DDR1) SODIMM-200 memory socket. The following sockets have been successfully tested with the module:

Tyco Electronics SODIMM Socket

<http://www.tycoelectronics.com>

Description:

- Plug height: 5.2 mm
- Max. main board component height below the module: 1.0 mm

→ Article number 1473005-1

Description:

- Plug height: 9.2 mm
- Max. main board component height below the module: 5.0 mm

→ Article number 1612618-1

NEXUS COMPONENTS

[www.nexus-de.com](http://www.nexus-de.com)

Description:

- Plug height: 5.2 mm
- Max. main board component height below the module: 1.0 mm

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→ Article number 5214HB52

Description:

- Plug height: 9.2 mm
- Max. main board component height below the module: 5.0 mm

→ Article number 5214HB52

Foxconn Electronics Inc.

<http://www.foxconn.com>

Description:

- Plug height: 5.2 mm
- Max. main board component height below the module: 1.0 mm

→ Article number AS0A426-E2SN-7F

### 5.3.2 JTAG FFC cable

Würth Elektronik 0.50 mm flat flexible cable Type 1 WR-FPC

→ Article number 687 610 050 002

<http://www.we-online.com>

Molex 0.50mm flat flexible cable Type A

→ Article number 982660097

<http://www.molex.com>



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### **5.4 Temperature range**

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C

**Table 27: Temperature range**

**Product:**     **DHCOM AM35xx Module**   Created by KH

Date of creation: 30. September 2011

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 [www.dh-electronics.de](http://www.dh-electronics.de)

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### **6 RoHS conformance**

This device has been manufactured RoHS compliant.



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### **Abbreviations**

AUDMUX	Audio Multiplexer
BSP	Board Support Package
CSI	CMOS Sensor Interface
CSPI	Configurable Serial Peripheral Interface
FFC	Flat Flex Cable
MBC	must be connected
PD	Pull-Down
PU	Pull-Up
SSI	Synchronous Serial Interface
USB OTG	USB On-The-Go